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On January 13th, GLOBALFOUNDRIES and Chartered finalized integration and emerged as the new GLOBALFOUNDRIES.

As the former manufacturing arm of AMD, we possess tremendous assets in our leading-edge manufacturing and technology capabilities. With the integration of Chartered Semiconductor, GLOBALFOUNDRIES achieves scale as one of the world’s largest foundries by revenue, differentiated by unmatched technology leadership with our flexible and collaborative approach to customer service.

The company’s leading edge capacity will expand to 5.8 million 200mm equivalents, including leading edge 300mm fabs on three continents.

With a global workforce of approximately 10,000 employees, GLOBALFOUNDRIES offers a new platform for innovation to drive the current and future generations of semiconductor products.

Introducing the World’s First Truly Global Foundry

Welcome to the World of the New GLOBALFOUNDRIES ... the New Leader in Technology, Globally Distributed Capacity, and Flexible Customer-centric Services.
ACCELERATE THE GROWTH AND INCREASE THE RETURN ON INVESTED CAPITAL OF THE GLOBAL SEMICONDUCTOR INDUSTRY BY FOSTERING A MORE EFFECTIVE FABLESS ECOSYSTEM THROUGH COLLABORATION, INTEGRATION AND INNOVATION.

▪ Address the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging

▪ Provide a platform for meaningful global collaboration

▪ Identify and articulate market opportunities

▪ Encourage and support entrepreneurship

▪ Provide members with comprehensive and unique market intelligence
Differentiation and time-to-market have always been the cornerstones of success for chip companies. Embedded Flash has played an important role in enabling competitive products by providing flexibility and a higher level of integration to the system-on-chip (SOC). At 90nm and above, embedded Flash is prevalent in many applications, ranging from code storage in power window controllers to secure key storage in smartcards. But at 65nm and below, there is currently no viable embedded Flash solution available. A solution will be needed as products migrate to more advanced process geometries in the next few years. In this article, possible non-volatile memory (NVM) technologies to enable embedded Flash at 65nm and below will be explored, including magnetoresistive random access memory (MRAM), silicon-oxide-nitride-oxide-silicon (SONOS), resistive random access memory (RRAM) and antifuse.

The traditional embedded Flash based on floating gate technology is not economically scalable below 90nm. New array architectures and process modifications will be required because the decreased oxide thickness in advanced technologies does not favor data retention in charge-trapping technologies such as floating gate. Process modifications may take years to optimize and may not be economically feasible in the more advanced processes. To augment the void in advanced process technologies, external serial Flash solutions have increased in popularity; their low pin count and small packaging can provide designers an alternative for code storage needs. The tradeoffs are the increased bill of materials (BOM) for the system; additional components, such as power supplies, to support the serial Flash; and reduced performance due to the relatively slow serial peripheral interface (SPI). For mobility products such as portable media players (PMP) or smartphones, where the form factor is shrinking and functionality is increasing, integration of the external serial Flash is beneficial for cost and performance. An embedded NVM solution is needed at 65nm and below. MRAM, SONOS, RRAM and antifuse are possible contenders. Cell size, density, scalability, read performance, program performance, array efficiency, added cost, endurance, erase time, data retention and high-volume mass production status are benchmarked in Table 1.

### Table 1. Comparing MRAM, SONOS, RRAM and Antifuse Technologies

<table>
<thead>
<tr>
<th></th>
<th>MRAM (Spin Torque)</th>
<th>SONOS</th>
<th>RRAM</th>
<th>Antifuse</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Size (F²)</td>
<td>10-30</td>
<td>10-15</td>
<td>6-20</td>
<td>10-70</td>
</tr>
<tr>
<td>Density</td>
<td>Up to 256Mb</td>
<td>Up to 2Mb</td>
<td>Up to 64 Mb</td>
<td>Up to 20Mb</td>
</tr>
<tr>
<td>Scalable</td>
<td>Limited, Write Current Increases with Scaling</td>
<td>Up to 40nm</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Read Performance (MHz)</td>
<td>75-125</td>
<td>20-50</td>
<td>20-100</td>
<td>15-100</td>
</tr>
<tr>
<td>Program Performance</td>
<td>Fast</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Array Efficiency</td>
<td>40%-60%</td>
<td>30%-50%</td>
<td>40%-60%</td>
<td>40%-60%</td>
</tr>
<tr>
<td>Added Cost</td>
<td>At Least +3 Mask Layers</td>
<td>At Least +8 Mask Layers</td>
<td>At Least +3 Mask Layers</td>
<td>No Additional Mask</td>
</tr>
<tr>
<td>Endurance</td>
<td>&gt;10K</td>
<td>10K</td>
<td>&lt;1000</td>
<td>&lt;1000 (Emulated)</td>
</tr>
<tr>
<td>Erase Time</td>
<td>Fast</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Data Retention</td>
<td>&gt;10 Years</td>
<td>&gt;10 Years</td>
<td>&lt;1 Year</td>
<td>&gt;10 Years</td>
</tr>
<tr>
<td>High-volume Mass Production</td>
<td>5-10 Years Away</td>
<td>Now</td>
<td>5-10 Years Away</td>
<td>Now</td>
</tr>
</tbody>
</table>

**MRAM**

MRAM has been under development since the 1990s. It is one of the earliest “universal memory” candidates. It is non-volatile and was touted to have the capacity and cost benefit of DRAM and the fast programming and random access of SRAM. The first-generation MRAM technology had technical challenges, including a program disturb mechanism that prevented manufacturability for mass production. The MRAM bit cell consists of one magnetic tunnel junction (MTJ) and a read transistor. The MTJ consists of two ferromagnetic plates, each of which can hold a magnetic field,
separated by a thin insulating layer. One plate is magnetized to a fixed polarity; the other can change through an external field to determine the state of the bit cell. A strong electrical current is driven along the plates to produce the magnetic field to program the MRAM. The change in magnetic polarity is sensed as a resistance change in the tunnel junction. The problem is that all of the neighboring storage elements are exposed to the same fields, resulting in unwanted programming. In addition to stability issues, the first-generation MRAM was not scalable. The thermal stability of the MTJ degrades as the spatial volume decreases.

Given the stability and scalability issues, most MRAM developers abandoned the first-generation technology. The leading second-generation technology is spin torque, also known as spin-transfer torque MRAM (STT MRAM). STT MRAM is programmed with an electrical current, not an applied magnetic field as was used in the first-generation MRAM. The electrical current must be spin polarized which is achieved by passing the current through a thin magnetic film or polarizer that is added onto one of the MTJ’s ferromagnetic plates. Data programming is performed by using the spin-polarized current to change the magnetic orientation of the storage element. Program disturb effects are minimized since writing is isolated to the selected MTJ device. The difference in the resistance of the MTJ device determines the state of the memory. The program speed is fast in STT MRAM, but the endurance is not as good as in the first-generation MRAM because there is a wear out mechanism; a thin tunneling layer is created during the spin torque magnetization when current is passed through the cell. Nevertheless, STT MRAM is promising with benefits of small cell size and high performance.

The challenges facing deployment of STT MRAM include proving the stability of the technology for mass production and managing the cost adder in addition to potential multi-site wafer handling. Embedded MRAM requires additional process steps, including depositing the polarized material. This is done in another facility because of fear of contamination to the logic process. For mass production, having multi-site processing may be a logistical nightmare. At least another seven to 10 years is ahead in development and innovation of STT MRAM to bring it to mass market.

SONOS

NVM technology based on the SONOS structure was introduced in the 1970s. It is a close relative to floating gate technology. Instead of charge trapping in the polysilicon layer, charge is trapped in the silicon nitride layer. There are N-channel based and P-channel based SONOS devices. The bit cell is formed from a standard polysilicon NMOS and PMOS transistor with the addition of a layer of silicon nitride added inside the transistor’s gate oxide; this is the ONO stack. The nitride is non-conductive but can trap and hold electrostatic charge. The nitride is electrically isolated from the surrounding transistors. Programming is achieved through channel hot electron injection or channel hot hole-induced hot electron injection or Fowler Nordheim (FN) electron tunneling or source side injection depending on the SONOS cell structure. Erase is achieved with FN electron tunneling or band-to-band injection of holes.

SONOS technology has made advancement resulting from the refining of the ONO stack. The ONO thickness has decreased dramatically in the last three decades, from 500 angstroms to around 100 angstroms. With the resultant decreased thickness, the programming voltage has decreased significantly from 30V to about 10V. With decrease bit cell size and programming voltage, higher capacity is possible. Discrete SONOS solutions will be more prevalent in addressing the short fall of floating gate scalability for NOR and NAND Flash. SONOS solved the charge loss issue seen in floating gate technologies but has the opposite problem of having strongly trapped electrons in the ONO stack that cannot be removed. Over time, the trapped electrons may not be able to be removed, creating a permanent programmed bit.

The relatively high programming voltage requires the addition of high-voltage devices to the standard CMOS process, increasing the area and, more importantly, adding extra mask layers and processing steps that make it a potentially expensive solution for embedded NVM.

RRAM

RRAM has thrown its hat in the ring as a “universal memory” candidate. Of all the candidates, RRAM is the newest. Research started in 2000 when it was discovered that an electrical pulse can induce resistive change in thin film materials, including chalcogenide glasses, perovskites and silicon dioxide. There are numerous theories proposed for the memory mechanism in RRAM. Examples include the alignment of oxygen vacancies in oxides, oxidation and reduction in perovskites, and the formation of metal filaments in chalcogenide glasses. RRAMs come in both unipolar and bipolar varieties. The unipolar device can be both programmed and erased with the same voltage polarity, while bipolar devices require opposite polarities to program and erase.

The advantages of RRAM are its fast access time (<10ns), low programming current (~10uA), and numerous materials that show hysteresis (memory) behavior. With these advantages, many companies from around the world have jumped onto the RRAM bandwagon. But initial findings on many of the RRAM types have shown poor endurance (~1,000 cycles), poor retention (~1 year), and a limited understanding of the mechanisms involved. Even the limited reports of better results have been on single cells or very small arrays, so the biggest challenge will be to prove RRAM in mass production. There may be another five to 10 years of development ahead before RRAMs could go into widespread commercial usage.

Antifuse

Antifuse has been around as long as SONOS. An antifuse is opposite of an electrical fuse. In the case of antifuse, the circuit is initially shorted (low resistance), and the application of electrical stress causes it to open. Antifuse NVM has been implemented for decades, and since 2001, it can be implemented in a standard CMOS process without additional processing steps. This technology is being used in products in mass production.

Figure 1. Antifuse Bit Cell with a Program Transistor and a Select Transistor

A hard gate oxide breakdown is used as the one-time programmable (OTP) NVM mechanism. The breakdown is achieved
Actel’s (NASDAQ: ACTL) low-power ProASIC® and ProASICPLUS® field-programmable gate array (FPGA) families have been designed into flight-critical applications on the new Boeing 787 Dreamliner commercial airliner. Flight computers, cockpit displays, engine control and monitoring systems, braking systems, safety warning systems, cabin pressurization and air conditioning systems, and power control and distribution systems all make use of Actel's highly reliable Flash-based FGAs.

Advanced Micro Devices (AMD) (NYSE: AMD) introduced the ATI Radeon™ E4690 mobile Peripheral Component Interconnect (PCI) Express Module (MXM) for graphics-intensive embedded systems. The industry-standard MXM 3.0 specification for graphics subsystems calls for reduced power, improved cooling capability and a lower z-height, enabling designers to create smaller, more efficient embedded systems and speed time-to-market. The ATI Radeon E4690 MXM features more than triple the 3D graphics performance of previously available solutions with low central processing unit (CPU) utilization and brilliant picture quality.

austriamicrosystems (SWISS: AMS) selected the AS3693A and AS3693B light-emitting diode (LED) driver ICs for TV models introduced at the Consumer Electronics Show (CES) 2010 in Las Vegas, Nevada. The innovative AS3693 family helps facilitate extremely flat liquid crystal display (LCD) TVs with the highest possible contrast ratios, resulting in outstanding picture quality. A patented power-saving technology actively regulates the LED power supply and minimizes power dissipation in the system.

Bourns' expanded product portfolio offers enhancements to the company's industry-leading components such as guitar potentiometers, commercial panel controls, slide potentiometers and rotary encoders to meet the professional audio market demand. Bourns is committed to provide the professional audio market with high-quality components for reliable sound.

Broadcom (NASDAQ: BRCM) introduced highly integrated digital terrestrial converter box system-on-chip (SOC) solutions designed for Japan's upcoming transition to digital TV broadcast transmission. Featuring an Integrated Services Digital Broadcasting -Terrestrial (ISDB-T) tuner, Broadcom's highly integrated, single-chip solutions address Japan's analog broadcast shut-off program, and meet the requirements for ISDB-T digital programming worldwide via cost-effective, low-power chip solutions.

Addressing emerging consumer electronics applications and the increasing demand for high-definition (HD) content, C2 Microsystems introduced the CC1200 full HD media processor family for broadband-connected set-top-box and digital TV applications. The CC1200 family is designed for the most demanding rich media applications that require full HD video decoding and presentation in conjunction with high-performance applications processing.

Cypress Semiconductor (NASDAQ: CY) announced that its TrueTouch™ touchscreen solution implements the touchscreens for new KDDI mobile phones manufactured by Sharp Communication Systems Group. The SH003 phone offers a 12.1-megapixel camera and leverages the TrueTouch solution to deliver user-friendly multi-touch gestures to manipulate photo images and control other functions.

Dialog Semiconductor’s (FWB: DLG) DA9035 IC for power management and audio was designed into LG Electronics’ GW880 smartphone. This design-in is the latest in a series of LG 3G mobile platforms to benefit from Dialog’s chips over the past 12 months.

Discera raised $11 million in a Series D financing round. The round was led by initial investors Scale Venture Partners, Horizon Ventures and Ardesta, as well as Lurie Investments, the private investing arm of the Ann and Robert H. Lurie Foundation.

eSilicon successfully took the Achronix Speedster 1.5GHz FPGA to commercial production. Achronix selected eSilicon to leverage the company’s world-class physical design and supply chain expertise. The first member of the Speedster family, the SPD60, is currently in production on TSMC’s 65nm G-Plus process technology.

Exar (NASDAQ: EXAR) released the industry's fastest (52Mbps) single-chip multi-protocol serial transceiver, the SP510. The transceiver supports high-speed data traffic, leading industry interface standards, adjustable logic-level flexibility (eliminates unnecessary discrete components) and has outstanding electrostatic discharge (ESD) protection. These characteristics and other advanced features make the product ideal for routers, frame relay, wide area network (WAN) access, voice-over Internet protocol-private branch exchange (VoIP-PBX) gateways, amongst others.

Fresco Microchip added the FM115, the industry's first single-chip global receiver for hybrid television, to its field-proven FM1100 family. The FM115 sets a new benchmark for superior broadcast reception and advanced design flexibility while significantly lowering system solution costs. The company's chips are featured in the latest tuner modules designed by several of the world's leading and largest TV tuner manufacturers, including LG Innotek, the world's largest tuner manufacturer; Panasonic Electronic Devices, the world's quality leader for consumer electronics; and NuTune, the largest independent tuner manufacturer.

GigOptix’s (OTCBB: GGOX) GX3440, a 45G differential limiting amplifier, is now shipping in full production. The GX3440 was designed to be used in 40G differential phase-shift keying (DPSK) and 40G differential quadrature phase-shift keying (DQPSK) telecom receivers, and can also be used in numerous instrumentation applications. It is the first of GigOptix’s family of differential and transimpedance amplifiers to be released to production that comprehensively addresses customers' requirements for telecom and datacom receiver amplifier solutions.

Himax Technologies (NASDAQ: HIMX) introduced infinity color technology (ICT), an innovative and proprietary image processing technology which enables significant power saving for thin-film transistor (TFT)-LCD TVs and monitors, regardless of cold cathode fluorescent lamp (CCFL) or LED backlights, while enhancing image quality.

IBM (NYSE: IBM) expanded the technology and business of its LotusLive cloud collaboration platform through a new research and development (R&D) pipeline from IBM Research and plans to open the LotusLive suite to new partners. LotusLive cloud services provide integrated e-mail, Web conferencing, social networking and collaboration with IBM's focus on security, reliability and enterprise integration.

Infinion Technologies AG (FSE: IFX) announced sample delivery of SMART™ UE2, the latest generation multi-band High-Speed Packet Access (HSPA)/Enhanced Data Global System for Mobile Communications (GSM) Evolution/General Packet Radio Service (HSPA+/EDGE/GPRS) radio frequency (RF) transceiver for mobile devices. Its groundbreaking digital architecture reduces the number of power amplifiers from five to one and integrates all low-noise amplifiers (LNAs) and interstage filters.

Integrated Device Technology (NASDAQ: IDTI) premiered the next-generation Hollywood Quality Video™ (HQV) Benchmark DVD. The de-facto industry standard test disk has been used by journalists, reviewers and consumers worldwide as a trusted source for evaluating the picture quality, processing
and performance of standard definition and HD products, including displays, DVD and Blu-ray players, audio/video (A/V) receivers, projectors and video processing boxes.

Jennic released its active radio frequency identification (RFID) reference design platform, providing a comprehensive solution for monitoring and tracking assets. Based upon Jennic's proprietary JenNet networking solution, the platform allows low-power wireless technology to be evaluated for active RFID tags in an asset management application.

LSI (NYSE: LSI) and Wichita State University (WSU) opened the Center for Storage Networking Research (CSNR) at the WSU campus. The CSNR represents collaboration between industry and academia to facilitate state-of-the-art theoretical and experimental research in storage networking. The research will focus on storage system advancements in areas such as performance, scalability, energy efficiency and security, and will potentially influence the design and evolution of future data storage systems.

Skiff and Marvell (NASDAQ: MRVL) released Skiff's reader development kit (RDK), which is designed to enable manufacturers to more easily create innovative reading devices with various display sizes, faster performance and reduced overall component costs. It does this by leveraging the world's first eReading SOC with an integrated electronic paper display (EPD) controller.

Microsemi (NASDAQ: MSCC) announced that the Defense Supply Center, Columbus (DSCC) qualification has been granted for its 200V, 400V and 600V family of Military Performance Specification (MIL-PRF)-19500/590 ultra-fast rectifiers in a compact thermally matched glass package. Microsemi's MIL-PRF-19500/590 rectifiers maintain ultra-fast switching characteristics even at extremely high temperatures.

MindSpeed Technologies (NASDAQ: MSPD) announced that TeamFli's Secure Gateway Solution (SGS) is now available on MindSpeed's Concerto 1000 packet processor, enabling a new class of multi-service business gateways (MSBGs) and other converged appliances.

NetLogic Microsystems (NASDAQ: NETL) was awarded its 400th United States patent. NetLogic Microsystems' portfolio includes over 600 worldwide patent issuances and pending filings. These achievements mark a significant milestone in the company's history of being at the forefront of technological and innovation leadership in high-performance semiconductor solutions that perform highly differentiated tasks for advanced 3G/4G mobile wireless infrastructure, data center, enterprise, metro Ethernet, edge and core infrastructure networks.

NXP Semiconductors agreed to license and deploy a hardware intrinsic security (HIS) solution in its next-generation SmaartMX® security chip technology. The partnership enables NXP to utilize Intrinsic-ID's Quiddikey™ solution to secure SmaartMX-powered assets against cloning, tampering, theft-of-service and reverse engineering.

On Semiconductor (NASDAQ: ONNN) introduced a family of low-side protected metal-oxide semiconductor field-effect transistors (MOSFETs) that feature high levels of integrated protection. Qualified in accordance with the Automotive Electronics Council (AEC)-Q101 standard, devices in the NCV840x family are ideal for use in switching applications operating in harsh automotive and industrial environments.

Open-Silicon acquired Silicon Logic Engineering (SLE) to enhance the company's derivative IC design capabilities. As part of Open-Silicon, SLE will increase the front-end capabilities for designing derivative ICs, which are increasingly in demand as semiconductor companies look to maximize the returns on their initial platform IC investments.

Plessey Semiconductors started trading from its semiconductor manufacturing facility in Roborough, Plymouth, UK. The Roborough fab currently produces 8-inch wafers for external customers on 0.35μm CMOS processes. Plessey Semiconductors was created from the acquisition of X-FAB and existing key engineering competence within a design and technology center located in Swindon, UK.

PLX Technology (NASDAQ: PLXT) exceeded shipping one million units to global customers. This landmark achievement validates broad consumer market adoption of PLX network-attached storage (NAS) solutions and reflects the rising demand of easily accessible, reliable and secure digital storage in the home.

Qualcomm (NASDAQ: QCOM) was ranked 9th on the 13th annual 100 Best Companies to Work For list by FORTUNE. To pick the 100 best companies, FORTUNE partners with the Great Place to Work Institute to conduct the most extensive employee survey in corporate America.

RF Micro Devices (NASDAQ: RFMD) commenced pre-production shipments of high-performance gallium nitride (GaN)-based cable television (CATV) hybrid amplifiers to a major U.S.-based CATV equipment provider. Operators of hybrid fiber coax (HFC) networks are installing fiber capacity deeper into their networks (“fiber deep” networks) to address the increasing demand for higher throughput video and broadband services.

LG Electronics selected SanDisk (NASDAQ: SNDK) 64GB SanDisk pSSDTM Gen2 as the solid-state drive (SSD) of choice for its new ultra-thin mobile PC. Unlike conventional hard disk drives (HDDs), SSDs have no moving parts, improving durability which helps prevent data loss resulting from drive failure.

Google's Nexus One mobile phone is leveraging several of Skyworks Solutions' (NASDAQ: SWKS) highly integrated power amplifier modules. These 3G solutions were incorporated in the Google platform as part of HTC's reference design.

Teknovus announced the availability of the TK3401, the intelligent Ethernet passive optical network (EPON) node controller. The TK3401 SOC facilitates evolution of the PON network by extending central office optical line terminal (OLT) to subscriber optical networking unit (ONU) distances up to 100km and by supporting connections to over 1,000 subscriber ONUs while supporting remote management, configuration and upgrade, protection switching and low-power operation.

Telegent Systems' analog mobile TV receiver was incorporated into two code division multiple access (CDMA) TV handset designs introduced in Q4 2009 by MobilMAX. With these designs, MobilMAX brings together its expertise in CDMA and GSM technologies and operator-grade solutions with a free-to-air TV feature that enables consumers to view the same live TV programming that they watch on conventional TV sets.

The GSM Association (GSA) selected Ubibidye as a finalist for the Global Mobile Awards in the Best Network Technology Advance category for its development of the world’s first antenna embedded radio for wireless communications. Ubibidye’s antenna embedded radio integrates all the RF elements of the network directly into the antenna housing. The product, which is compatible with current and next-generation standards, completely eliminates the need for coaxial feeder cables, remote electrical tilt systems and additional amplifiers on antenna towers and masts.

Vixs Systems announced that Sony selected its XCode™ 3106 for the latest line of Vaio L multimedia PCs. The XCode™ 3106 provides advanced features such as HD transcoding of HD MPEG2 broadcast video to a HD MPEG4 Advance Video Coding (AVC) format for increased video storage. Video storage on the local HDD has increased by four times, as compared to a non-transcoding mode.

Wolfson Microelectronics (LSE: WLF) introduced the WM8595, a world-leading multi-channel audio codec designed to offer a complete high-performance audio solution in an ultra-thin package for consumer products, including HD digital televisions, DVD recorders and Blu-ray players.

Xilinx (NASDAQ: XLNX) announced the first shipments and availability of its Virtex-6 LX760 device. As the industry's largest FPGA available for delivery with immediate design tool support, the Virtex-6 LX760 device enables Xilinx customers who need raw logic density and industry-leading input/output (I/O) performance to get started on their projects today using the Xilinx ISE Design Suite 11.4.

Zoran's (NASDAQ:ZRAN) VaddisHD™ processor enables playback of HD video in JVC's new HD media player models CU-VS100 shipping to the U.S., Europe and Asia. JVC's new HD media player allows consumers to play their HD camcorder content on any television set.
For large amounts of on-chip code and data, mask read-only memory (ROM) provides an inexpensive and easily programmed storage mechanism. However, the inability to configure ROM after wafer processing means that information stored in the ROM cannot be changed in the field.

Antifuse one-time programmable (OTP) provides a flexible, field-programmable alternative to ROM. An antifuse-based bit cell uses controlled, irreversible thin (gate) oxide breakdown to program a bit. Un-programmed, the bit cell looks like a capacitor; but when the oxide is ruptured, there is a conductive path which exhibits current flow several orders of magnitude higher than that for an un-programmed bit.

Antifuses program by applying a high-voltage pulse not encountered during normal operation across the gate and substrate of the thin oxide transistor (around 6V for a 2nm-thick oxide or 30MV/cm). This breaks down the oxide between gate and substrate. This programming voltage can be supplied externally or with an embedded charge pump. The positive voltage on the transistor’s gate forms an inversion channel in the substrate below the gate, with the high electric field inducing a tunneling current to flow through the oxide. This current produces traps in the oxide, increasing the current through and, ultimately, melting the oxide, which then forms a conductive channel from gate to substrate. A current density of 100μA/100nm² forms the conductive channel with the breakdown occurring in, typically, 100μs or less.

There are several reasons why field-programmable OTP makes sense. First, the chip designer can commit to silicon prior to code completion. This feature accelerates product time-to-market. The flexibility of being able to try different versions of code and to perform side-by-side comparisons of the code versions allows software developers to optimize code for a particular design. Finally, field-programmable OTP also supports a chip design that can have additional features that may not be available on initial silicon, but can be added in later versions of the chip.

One chip can also have several variants, which simplifies inventory and allows a single chip to support multiple versions of a feature set. This is useful, for example, in an application such as an entertainment system for an automobile family where different car models within that family have different levels of audio requirements. Another example would be implementing a chip supporting several communications protocols such as a network chip supporting Bluetooth and Wi-Fi. In a given application, the chip is enabled to support either one or both of these protocols using antifuse-based OTP in place of ROM to do the specific enablement.

When investigating embedded field-programmable OTP for a chip design, be aware that different products (having different bit cell architectures) on the market have varying characteristics, as is the case for any embedded memory intellectual property (IP). The best antifuse OTP architecture provides memory IP that is very dense, has a fast read access time, and supports easy conversion from the OTP macro to mask ROM for cost reduction during production.

### 1T vs. 2T Antifuse OTP Bit Cell

There are two basic oxide breakdown antifuse OTP architectures available – two transistors (2T) per bit cell and one transistor (1T) per bit cell.

An inherent problem with a 2T antifuse bit cell is predicting where the conductive programming channel will be located. Three potential regions exist where the oxide breakdown occurs: above the transistor channel, to a leakage control implantation or to the lightly doped drain (LDD) diffusion. This variability compromises the reliability, yield and portability between processing facilities of arrays using the 2T antifuse bit cell since the bit cell read and programming characteristics vary between these different regions.

A split channel (1T) metal oxide semiconductor (MOS) antifuse bit cell eliminates the diffusion area from the thin oxide transistor, ensuring programming in the normal transistor channel region. This produces a bit cell exhibiting more consistent programming and read characteristics. In addition, the 1T bit cell, not much larger than a mask ROM bit cell, consumes significantly smaller area than a 2T bit cell. This area reduction increases overall chip yield and decreases cost, particularly for large memory blocks. Furthermore, a 1T bit cell exhibits very fast read access times, as low as 10ns for advanced process nodes, ports more readily between foundries and scales easily with process node shrinks.

### OTP vs. ROM

Using 1T antifuse OTP in place of ROM does require slightly more
area. In addition, the programming time OTP requires increases approximately linearly with bit count. While ROM is programmed during chip fabrication, there is no programming time or cost; however, the ROM still needs to be tested to verify its contents. While these OTP considerations are not very important for small bit count applications, they are at high bit counts, for example, when the OTP is storing hundreds of thousands of bits of boot code or firmware. Programming and verifying OTP will result in additional test time.

These OTP factors are acceptable at a prototype phase of chip development, but may become too expensive during production, especially for high bit count applications. However, the ability to complete code development during silicon fabrication and make and test code changes during prototyping, coupled with the ability to accelerate market entry and reduce final product cost, provides a compelling argument for using field-programmable OTP during product development.

**ROM Conversion**

Designers need to consider the ease of converting the OTP macro to ROM when evaluating an antifuse-based OTP memory architecture.

For some OTP architectures, conversion to mask ROM requires a single graphic data system (GDS) layer change—diffusion (thin gate oxide)—within a standard process flow. Many customers do their prototype development using multi-project mask sets to cost-share the mask set with other developers. When they go into production, they then purchase a production-quality mask set anyway, so they do not incur any incremental costs of this layer change. Accelerating product time-to-market often justifies the added mask cost for changing to ROM should a customer already use a dedicated mask set while providing a cost-reduction path.

There are many benefits of converting either all or part of an OTP macro to mask ROM once all or part of the bit storage is frozen. First, there is significant cost savings due to the reduced time for automatic test equipment (ATE) programming of the macro. The memory footprint does not change when converting field-programmable 1T OTP to mask ROM, minimizing non-recurring engineering (NRE) costs for layout.

With a 1T bit cell architecture, designers may “mix and match” OTP and ROM in the same macro for many applications, such as factory or field trimming of analog circuitry and sensor conditioning; product customization (one silicon chip with several variants) where functionality is enabled by OTP programming; chip identification, lot date coding and other identification functions; future code patching; and end-customer personalization such as that required for digital hearing aids and implanted medical devices.

**Security Considerations**

An additional advantage of antifuse OTP in place of ROM is the extra security it provides for stored data or code. Reverse engineering (via de-processing) a ROM bit will easily determine whether the memory cell is storing a 1 or a 0. It is virtually impossible to determine the content of an antifuse OTP bit cell, either by physical de-processing or by voltage scanning after removing the top layers of the chip. Since the antifuse bit cell does not use stored charge to determine whether it contains a logical 1 or 0, scanning the cell will not reveal its contents.

If a memory macro contains both ROM and antifuse OTP, creating an encryption key in OTP for decrypting the ROM will help assure security of the ROM's contents since the key is inherently secure.

**Example**

The following example shows a 128Kbit (8K x 16) OTP macro used for storing code. 112Kbits of code storage have been finalized and the macro section with this stored code converted to ROM. The remaining 16Kbits of field-programmable OTP are reserved for future code development by the end-product manufacturer. After the ROM conversion, the programming time for this macro is reduced by 87.5 percent.

![Figure 2. Split Channel OTP to Mask ROM Conversion](Image)

A split channel antifuse OTP bit cell supports a very simple conversion to mask ROM, with only a single GDS layer change (for diffusion) and no variations from a standard process flow.

![Figure 3. Partial Conversion of an OTP Array to ROM](Image)

The ability to convert part of an antifuse OTP array to ROM substantially reduces ATE time and cost for arrays programmed during test while leaving some field-programmable memory for future trimming, chip ID, code updates or other purposes.

**About the Authors**

Jim Lipman is currently director of marketing at memory IP provider Sidense. Prior to Sidense, Jim worked at Cain Communications as vice president of client services, TechOnLine as content director, and at EDN Magazine as application-specific IC (ASIC) and electronic design automation (EDA) editor. He also was employed by VLSI Technology, where he held various training, marketing and public relations positions, and did chip designs at both Hewlett-Packard and Texas Instruments earlier in his career. Jim received his B.S.E.E. and M.S.E.E. degrees from Carnegie-Mellon University in Pittsburgh, Pennsylvania and his doctorate in electrical engineering from Southern Methodist University in Dallas, Texas. He also has a Masters of Business Administration from Golden Gate University in San Francisco, California. Jim is a senior member of the IEEE. You can reach Jim Lipman at 925-606-1370 or jim@sidense.com.

Todd Humes brings over 20 years of engineering and management experience to Sidense, where he is the vice president of product engineering. Following the acquisition of Impinj’s IP group, he was senior director of engineering at Virage Logic for the embedded NVM group. Prior to working at Virage Logic, Mr. Humes joined Impinj at its inception and served as chief technical officer and, later, vice president of engineering for IP products. Mr. Humes was also responsible for Impinj’s patenting efforts. Before Impinj, he held several management and engineering positions at TRW. Mr. Humes earned his M.S. in electrical engineering from the California Institute of Technology and B.S. in electrical engineering from California Polytechnic State University, San Luis Obispo, California. He currently holds 39 United States patents and has numerous U.S. and foreign patent applications. You can reach Todd Humes at 206-719-5361 or thumes@sidense.com.
**Dongbu HiTek** announced that it will manufacture low-frequency receiver ICs for Micro Analog Systems Oy (MAS), a fabless analog semiconductor company based in Espoo, Finland. The chips, manufactured at Dongbu HiTek’s world-class wafer fab using a specialized bipolar/CMOS/DMOS (BCDMOS) process at the 0.35μm node, will serve as a core component in global radio-controlled time-signal applications. According to Dongbu HiTek, MAS’ receiver chips are designed to enable accurate real-time capture of radio transmissions from time-signal stations around the world. The chip significantly captures time calibration data via low-frequency (long wave) transmissions regardless of the transmitter receiver’s location. As a result, low-frequency communications overcome limitations associated with the use of high-frequency (short wave) techniques.

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**Fujitsu Microelectronics**, a leading global semiconductor supplier, offers a wide range of process technologies, design solutions and advanced packaging services to customers. Customers can access the company’s CMOS process platforms, from 180nm to 65nm, and design intellectual property (IP) either through convenient full turnkey application-specific IC (ASIC) or cost-effective customer-owned tooling (COT) engagement. In addition, Fujitsu’s liquid crystal-on-silicon (LCOS) process technologies developed for emerging pico projector and electronic view finder applications are also available to COT customers. Fujitsu’s advanced packaging technology, including multi-chip modules and die stacking, is an ideal solution for applications where multiple chips are required to meet system requirements.

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**GLOBALFOUNDRIES** announced that it has officially integrated operations with Chartered Semiconductor Manufacturing and started functioning as one company under the GLOBALFOUNDRIES brand. The announcement marks the emergence of the new GLOBALFOUNDRIES, the world’s first full-service semiconductor foundry with a truly global manufacturing and technology footprint across Asia, Europe and the United States. The combined company employs approximately 10,000 people around the world, anchored by headquarters in Silicon Valley and advanced manufacturing operations in Singapore; Dresden, Germany; and a new leading-edge fab under construction in Saratoga County, New York. These sites are supported by a global network of research and development (R&D), design enablement, and customer support in Singapore, China, Taiwan, Japan, the United States, Germany and the United Kingdom.

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**Grace Semiconductor Manufacturing**, one of the leading semiconductor foundries for differentiated technologies, has successfully developed an advanced 45V lateral-diffused metal-oxide semiconductor (LDMOS) process for power management based on its stable 0.18μm logic baseline. Compared with legacy nodes, the 0.18μm logic baseline allows a much higher level of integration of digital circuits, fulfilling the requirements of system-on-chip (SOC) and smart power applications. Grace’s mature 0.18μm logic process offers customers a complete process design kit (PDK) with great model accuracy which significantly shortens design cycle time and therefore accelerates ramp-up. It also provides customers with alternative generic and low-power baseline options.

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**IBM** announced the availability of a variety of features and technologies aimed at helping clients drive circuit innovation in mobile handsets. The new offerings are part of IBM’s 180nm suite of analog/mixed-signal foundry technologies and are primarily focused on driving innovation and integration in the handset radio function. These features provide fabless clients the flexibility to create new architectures and circuit topologies to help reduce power, size and cost to meet the demands of 3G/4G multi-mode/multi-band handsets. They are a result of IBM’s collaborative innovation initiative in working with clients to bring game-changing technologies to the marketplace. The offerings complement IBM’s already rich set of technologies and aim to further enhance the 180nm node for additional market applications. The added features and enablement include thick copper (Cu) back-end metal levels, through-silicon via (TSV) technology, radio frequency (RF) silicon-on-insulator (SOI) programmable signal processor (PSP) models, an integrated passives technology (IPD5PaE) and 180nm-thick SOI technology (CSO17TF). Validated PDKs with the enhanced features are available today.
LFoundry is a leading analog and mixed-signal silicon foundry with a 200nm production line based in Landshut, Germany providing access to manufacturing services down to advanced analog 0.15μm CMOS technologies with innovative extensions. Based in the heart of Europe, LFoundry is in an excellent position to support a wide portfolio of applications, especially when it comes down to high flexibility and the customization of technologies.

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MagnaChip Semiconductor, a leading Asia-based designer and manufacturer of analog and mixed-signal semiconductor products for high-volume consumer applications, and Microsemi, a leading manufacturer of high-performance analog/mixed-signal ICs and high-reliability semiconductors, announced that they have partnered to develop advanced mixed-signal process technology that is optimized for products in Microsemi’s key commercial growth markets. The new process is electrically compatible with MagnaChip’s own 0.35μm baseline process that is already used by Microsemi to manufacture current products.

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Riding on the recent surge in the global demand of smartphones, SilTerra Malaysia’s advanced high-voltage technology is well positioned to capture this fast-growing market. The latest 0.11μm high-voltage process offers the finest static random access memory (SRAM) bit cell suitable for ultra high-resolution display in Half-size Video Graphics Array (HVGA), Noise Half Delta (nHD) and Wide Video Graphics Array thin-film transistor (WVGA TFT) panels. The CL110H32 technology features triple-gate oxides with five metal layers of aluminum interconnect. In addition, the technology offers asymmetry high-voltage well for denser design, one-time programmable (OTP) cell for gamma color tuning and voltage trimming, electrostatic discharge (ESD) protection circuitry, and metal capacitors design guideline. A complete foundry design kit (including design rules, models, PDK and design tool tech files) and design libraries (including standard cells, input/output (I/O) cells and SRAM) are now available for customers to start the design.

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With Taiwan Semiconductor Manufacturing (TSMC) adding a low-power process to its 28nm high-k metal gate roadmap in the last year, the company is closely working with customers and ecosystem partners to build comprehensive partnerships on the 28nm process node. The advanced process node enables more features to be integrated into smaller chips with a high level of cost efficiency, accelerating the expansion of wireless into new market segments. A recent deal was announced with Qualcomm, establishing a close relationship between the two partners on 28nm process technology.

The new process is expected to enter risk production in Q3 2010. TSMC’s 28nm development and ramp has remained on schedule since the company announced the technology in September 2008. The company plans to further discuss both 28nm and 40nm at the TSMC Technology Symposiums in April 2010.

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Tower and Jazz Semiconductor announced major achievements in the first year of their merger and launched a new company brand, TowerJazz, at its annual technology conference. Also, the foundry signed a definitive agreement with an Asian entity to provide know-how, training and turnkey manufacturing solutions at revenue of $130 million.

VT Silicon chose TowerJazz’s 0.18μm SiGe process for the world’s first fully integrated 4G RF front-end IC. As well, Phasor selected the foundry’s high-performance SiGe BiCMOS process for its innovative transceiver chipset for mobile broadband service on moving platforms.

TowerJazz was also selected as the preferred foundry by Korea’s C&S Technology for power automotive devices for Hyundai and Kia Motor Company.

CMOSIS announced it chose TowerJazz’s CMOS imaging process for its first off-the-shelf high-resolution sensor. In addition, National Aeronautics and Space Administration (NASA) selected TowerJazz and the Advanced Science and Novel Technology Company (ADSANTEC) for its Lunar Atmosphere and Dust Environment Explorer (LADEE) mission.

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United Microelectronics (UMC) began equipping its 300mm Fab 12i in Singapore for 40nm production, and will expand manufacturing capacity from 31,000 to 41,000 wafers per month in the coming months. This will be the foundry’s second 300mm fab with 40nm capabilities. The company is also re-defining the limitation of state-of-the-art 8-inch CMOS technologies with the aggressive development of aluminum back-end-of-line (Al-BEOL)-related technologies, leading the industry into a brand new era of diversified CMOS applications, including logic/mixed-mode (MM), RFCMOS, drain-extended metal-oxide semiconductor (DEMS), lateral-diffused metal-oxide semiconductor (LDMOS), conductor-insulator-semiconductor (CIS), microelectromechanical systems (MEMS), embedded memories, etc. These modern green technologies will enable new functionality and features for everyday applications.

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The X-FAB Group recently expanded its 0.35μm technology offerings with the first foundry technology optimized for Blu-ray and high-speed optical data communication applications. Dubbed XO035, the new 0.35μm process includes a unique blue PIN module which enables the design of high-performance photo detectors. The PIN diode offers the highest sensitivity for blue light in the market, about 0.31 Amperes per Watt, which is close to the physical limit. Available now, the XO035 is ideal for all applications for which high sensitivity and high bandwidth are crucial, such as photo detector ICs (PDICs) for Blu-ray and other optical data storage applications, optical data communication devices and high-dynamic range cameras.

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Perfect timing requires speed and precision, particularly in the noisy universe of digital chips...

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While price and density play large roles in selecting dynamic random access memory (DRAM), many other considerations must be taken into account. For example, long-term product support is a key consideration for many applications. Manufacturers of products with long product lifecycles, such as network infrastructure and automotive products, require lasting product support. The DRAM market’s transition to double data rate, third generation (DDR3) will have implications for many of these manufacturers.

In addition to long-term product support requirements, networking and automotive manufacturers also have stringent quality and wide temperature range requirements. With this in mind, some chip vendors are taking measures to improve product reliability and to widen supported temperature ranges.

For many handheld and mobile products, form factor and power consumption are key considerations. This is driving demand for known good die (KGD) DRAM that minimizes both active and standby power to extend battery life.

Ensuring Continuity of Supply

Many large DRAM suppliers are currently shifting production away from synchronous dynamic random access memory (SDRAM), DDR and DDR2 to DDR3. Market research firm iSuppli predicts that by the end of 2010 DDR3 will represent 71 percent of DRAM shipments in terms of gigabit-equivalent shipments. “With DDR3 commanding higher pricing than DDR2, memory makers realize where the big money will be in 2010,” said Mike Howard, senior DRAM analyst for iSuppli. “Because of this, they are more than willing to transition production to the new memory technology (DDR3).”

A major factor leading this transition is Intel’s latest microprocessor architecture, named Nehalem, which supports only DDR3 and is used in PCs and servers.

This transition to DDR3 has significant implications to markets such as networking, automotive, industrial and medical. Many of the designs in these markets currently use SDRAM, DDR or DDR2. They require sustained product support, in many cases 10 years or greater. They will need a DRAM supplier that can provide a consistent supply of SDRAM, DDR and DDR2 for many years.

Typical automotive systems have active production cycles lasting five years or more. Additionally, the development and validation phases must precede that by three to four years. Changes to systems are expensive and introduce potential bugs or problems to vehicle operation. This drives the automotive segment to require that a memory configuration be available for 10 years or longer.

Enhancing Long-term Reliability

In addition to stable product support, reliability is also a key consideration. Package reliability is a key determinant of product reliability. Some vendors are improving package reliability by taking steps such as introducing copper leadframes and nickel-palladium-gold (NiPdAu) plating material.

Better Joint Reliability

Parameters such as coefficient of thermal expansion (CTE) must be taken into account when reviewing package reliability. Different CTE for materials on a printed circuit board (PCB) can cause package-related problems such as stresses at solder joints. This is depicted in Figure 1. The different expansion rates cause pushing and pulling effects at the solder joint where the leadframe and the PCB interface.

The effects of this stress may accumulate to the point that a crack appears at the solder joint, causing an electrical discontinuity. Traditional thin small-outline packages (TSOPs) with Alloy42 leadframes can suffer from this problem. The reason for this is the devices likely would be mounted on a PCB with copper traces and landing pads. When the board is heated, the materials made of copper would expand more readily than those made of Alloy42. Some DRAM manufacturers are introducing copper leadframes for TSOPs to address this issue. A copper leadframe expands and contracts proportionally to the copper pads on the PCB, resulting in reduced stress on the solder joint. Additionally, copper leadframes improve package reliability by reducing thermal resistance. Improved thermal resistance results in better heat dissipation from the chip to the leadframe, and therefore less heat-related stress to the chip. Heat stress to the chip is one of the leading causes of a non-mechanical component failure in a long-life application.

Lead-Free Product and Whisker Prevention

The European environmental legislation known as Restriction of Hazardous Substances (RoHS) has driven the move to lead-free packaging. Without lead, the tin solder that electrically and physically connects components to boards can develop microscopic metal filaments known as whiskers. These whiskers can bridge metal contacts and cause a short circuit. Solutions such as annealed devices with matte tin plating material can be used to minimize the risk of whisker growth.
The electronics industry generally accepts an annealed matte tin plating solution. However, the International Electronics Manufacturing Initiative (iNEMI) lists NiPdAu as the preferred plating material, citing the further reduced risk for whiskers. Some DRAM suppliers use this type of plating for their copper leadframes, targeting systems with no tolerance for whisker potential.

While the overall trend is toward lead-free products, some demand for leaded products still exists. This request for leaded support is mostly for ball grid array (BGA) packages. The reason some companies still request leaded product is because they are reviewing statistical reports to ensure the long-term reliability of lead-free products. Thus, in some cases, markets such as networking/telecommunications and automotive, which have long-term product requirements, still require leaded support. Some companies have committed to supporting leaded BGA packages and TSOPs for the next few years.

**Automotive Memory Requirements**

Advancements in automotive electronic systems are allowing vehicles to become safer, more occupant-friendly and more fuel-efficient. For example, smart safety systems such as anti-lock braking systems (ABS), car cameras and radar systems have been introduced to help prevent collisions. Multifunction consoles offer music, Global Positioning System (GPS) navigation, Bluetooth communication, satellite radio, vehicle performance status and climate control. These advancements in electronic systems are aided by the use of memories such as DRAM to store and manipulate data. Automotive systems require DRAM to be very reliable and to operate across a wide temperature range.

**Reliability**

Problem-free vehicle operation is important to automakers because recalls are very costly both in terms of dollars and customer perception. This means any IC that is used in an automotive system needs to be very reliable.

To ensure high quality and reliability in harsh environments, an industry group called the Automotive Electronics Council (AEC) requires that IC manufacturers follow the AEC-Q100 specification. This specification is defined by the AEC as a “stress test qualification for integrated circuits.” The intent of the AEC-Q100 is to establish standards to ensure reliable, high-quality products.

Careful design of the package and choosing the right materials and process technology can help in meeting the AEC-Q100 specification. Additionally, device reliability can be enhanced by implementing dynamic burn-in which reduces early-life failure rates.

**Wide Temperature Range Operation**

Automotive applications require a wide operating temperature range typically from -40°C to 85°C, and in some cases up to 105°C. Therefore, DRAM targeted at this segment needs to be designed with this extended temperature range in mind. It must be able to maintain its performance over the extended temperature range. To help ensure performance over temperature, additional wafer sort testing can be done and more stringent yield limits can be placed. Also, a 100 percent final test across the temperature range can be conducted at the package level.

**Lower Power and Smaller Form Factors**

Mobile devices are moving to smaller form factors and higher levels of integration. Additionally, higher speeds and greater processing capabilities are making power consumption a key consideration for mobile devices.

### Smaller Packages with KGD

KGD allows for smaller form factors and greater levels of system integration. This is accomplished by stacking a KGD DRAM along with a system-on-chip (SOC) device in a multi-chip package (MCP) or system-in-package (SiP). This is shown in Figure 2.

![Figure 2. Example of a SiP](image_url)

**Achieving Lower Power**

Mobile or low-power SDRAMs provide options to improve both active and standby power. Reducing active and standby power extends battery life and improves system reliability. By taking system use into consideration, an engineer can select from the following power-saving options to provide low active and standby power:

- **Auto Temperature Compensated Self Refresh (ATCSR):** An on-chip temperature sensor controls the refresh rate based on die temperature. Higher temperatures require more frequent refreshing. By automatically adjusting the refresh rate, power consumption is reduced, especially at lower temperatures.

- **Partial Array Self Refresh (PASR):** PASR selects the amount of memory that will be refreshed during self-refresh operation. By eliminating unnecessary row activation, power consumption is reduced.

- **Deep Power Down (DPD) Mode:** DPD mode cuts power to the memory array and decreases leakage current. This provides the lowest power state when data retention is not required.

- **Programmable Output Driver Strength (DS):** DS allows the output drive to be programmable for full or partial output drive strength. For lighter loads such as those found in KGD applications, the drive strength can be lowered. Power consumption can be minimized by adjusting the output drive strength to match the actual bus loading.

**Beyond Price and Density**

Generally, when one thinks of DRAM, price and density first come to mind. However, depending on the application, many other considerations must be taken into account. Continuity of supply, long-term reliability, form factor and power consumption are also key considerations when choosing DRAM.

**About the Author**

Pat Lasserre is the director of strategic marketing for ISSI. He is a certified product manager from the Association of International Product Marketing & Management. He holds a B.S.E.E. from the University of California, Berkeley. You can reach Pat Lasserre at pat_lasserre@issi.com.
Advantest’s AccelerATE Solutions is a multi-platform test engineering service provider located in San Jose, California. The company’s mission is to leverage its extensive experience and contacts within the semiconductor test arena to expedite its customers’ time-to-market. AccelerATE provides the following services to reduce production costs: test pattern conversion, test interface development, test program development, device characterization, failure analysis (if required), test program optimization, sample production, deployment to volume manufacturing, and test program conversion.

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AdvanTEST’s T2000 system-on-chip (SOC) test platform offers the industry’s highest levels of multi-site and parallel testing capabilities, speeding time-to-volume economics for SOCs, including graphics processors, radio frequency (RF) SOC, cellular RF and digital baseband, power management and audio/video (AV) devices.

Silicon Valley’s fabless companies now have a gateway to volume production at STATS ChipPAC’s facilities in Asia. The T2000 SOC architecture features a loadboard user space more than five times larger than competing alternatives and the industry’s most advanced control architecture for the fastest test times, both at today’s multi-site levels and for future expanded site counts. The T2000 offers superior integration of high-channel density analog, direct current (DC) and RF instrumentation and the lowest cost digital instruments from 50Mbps through 6Gbps.

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Amkor Technology has had copper wire bonding qualified with customers since 2007 and in production since 2008. With the steep rise in gold prices over the last year, customer conversion to copper wire has accelerated across Amkor’s broad wirebond portfolio. Copper wirebond production ranges from Amkor’s low-wire density small outline (SO) family through high-wire density plastic ball grid array (PBGA) packages. With years of experience and high-volume data covering multiple factories, wafer nodes and package types, Amkor helps customers even in high-reliability applications take advantage of the cost benefits copper wire provides.

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Evans Analytical Group’s (EAG) release-to-production (RTP) team provides engineering service and support from chip tapeout to volume production. The company’s services include automatic test equipment (ATE) test hardware and software development, reliability qualification, electrostatic discharge (ESD) and latch-up, printed circuit board (PCB) design, circuit edit/debug, yield enhancement, failure analysis, electron microscopy, and equipment calibration and repair services.

EAG’s newly added ion mill cross-section capability enables the company to quickly and cleanly create large-area cross sections on a range of materials to aid in development and failure analysis efforts at the package or die level, including the characterization of through-silicon vias (TSVs), solder balls and bumps.

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LTX-Credence, a provider of innovative semiconductor ATE solutions, announced a new multi-channel, VI instrument for the ASL test system. The XVI greatly enhances multi-site capability for the ASL1000 and ASL 3000 test systems with 14 channels per board. The XVI provides extended power ranges, enhanced source and measure accuracy, and per-pin digitizer capability. All of these features will provide users with up to 40 percent faster test times compared to existing ASL VI instrumentation. The XVI can be purchased as an upgrade for the over 3,000 ASL testers in the field. Multiple domestic and Asian-based customers have purchased the XVI and are already using it in volume production applications.

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MVTS Technologies is a global full-service provider of refurbished ATE to the semiconductor industry. MVTS extends the life of legacy ATE by providing access to “out of production” used equipment, spare parts and services. With an extensive inventory and a wide range of products, MVTS positions itself as the ATE capacity partner to its customers.

MVTS now exclusively owns the rights to a selection of legacy Credence product lines and is offering used Credence legacy testers, refurbished and configured to customers’ specifications with an extended warranty. MVTS also offers used and refurbished LTX and Teradyne test equipment, spare parts and turnkey services as well as Verigy...
test application services.

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Presto Engineering, an ISO 9001 company, provides comprehensive semiconductor test and analysis solutions to integrated device manufacturer (IDM) and fabless companies, helping to improve the speed and predictability of new product releases. Presto combines unique technical expertise, extensive industry experience and state-of-the-art ATE, reliability, failure analysis and fault isolation capabilities to offer a complete product engineering solution designed to complement the internal resources of its customers.

Presto recently received a $2 million investment from Masseran Gestion in France and acquired certain capital assets of NXP Semiconductor. As of February, Presto opened a second product engineering services and testing hub in Caen, France and has established a subsidiary, Presto Engineering EUROPE.

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Quik-Pak provides IC packaging, advanced assembly and prototype services for fabless semiconductor companies, enabling faster time-to-market for new devices within a matter of an hour or a few days. Companies should make Quik-Pak a standard part of their package development and design verification process. The company’s open cavity plastic packages (OCPP) offer an array of endless possibilities with no minimum quantity required. When customers need a turn-key solution, Quik-Pak can do it all, from wafer dicing and backgrind, package procurement, custom BGAs and preparation to die attach, wirebonding (gold (Au), aluminum (Al) or copper (Cu)), flip-chip, encapsulation, molding and marking to deliver production-quality prototype parts for internal testing when time is critical. Quik-Pak is a division of Delphon Industries. Visit www.delphon.com to learn more.

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Scanmetrics will be introducing a design kit to use its Wireless Test Access Port (WiTAP™) non-contact test points, available through their Web site. The kit will allow designers to access internal test nodes for design verification and debug and to verify Scanmetrics’ non-contact test technology and chip-to-chip communications for 3D packaging. WiTAP™ enables cost savings by increasing productivity and revenue. The technology enables shrinking of input/output (I/O) pitch and die size while also offering increased access to internal or “hidden” test points in 3D packages. This allows designers to debug at a lower cost and more thoroughly, and to test earlier in the process, faster than with contact-based systems and more extensively for the same cost. Also, with proper design consideration, WiTAP™ can be used as an interconnect to replace TSVs for 3D packaging.

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STATS ChipPAC has ramped first-generation embedded wafer-level ball grid array (eWLB) technology to high-volume production. The eWLB technology provides solutions for semiconductor devices requiring a higher integration level and a greater number of external contacts. STATS ChipPAC has established a robust, automated eWLB manufacturing process that includes wafer reconstitution, wafer-level molding, redistribution using thin-film technology, solder ball mount, package singulation and testing. Incoming wafers in both 8-inch and 12-inch diameters can be supported, and no bumping is required as the package is essentially built on top of a reconstituted wafer. Typical applications for eWLB are baseband and RF products for mobile and consumer products.

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Teradyne introduced a new member of its Magnum family of memory test solutions, the Magnum 2x™. Capable of testing over 1,280 devices in parallel, the Magnum 2x delivers an unprecedented level of efficiency and low cost for probe and package test. While designed for massive parallel test applications, the Magnum 2x achieves speeds up to 800Mb/s for full performance testing of memory and logic devices. Teradyne has shipped multiple Magnum 2x test systems to major customers in the Pacific Rim. Based on the successful Magnum 2 architecture, the 2x continues the Teradyne legacy as the leader in low-cost, high-throughput testing with twice the pin count. Magnum 2x delivers the required flexibility allowing customers to choose the configuration that best fits their needs today and in the future. System configurations start with one chassis offering up to 1,280 pins; two chassis with up to 2,560 pins; four chassis with up to 5,120 pins; and eight chassis with up to 10,240 pins—each with the same small footprint as Magnum 2. Additionally, test engineers can run their existing Magnum 2 test programs on the 2x, resulting in significant savings of time, resources and test costs.

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Verigy, a premier semiconductor test company, won EDN magazine’s 2009 Hot 100 Product Award for its software toolset comprising the Triage Fault Locator™ and YieldVision™ analysis and visualization tools, which work together to form the company’s yield learning solution. Verigy is the only test equipment manufacturer to win in the software category. The yield learning solution facilitates design for manufacturability (DFM) by providing the accuracy necessary in product development labs as well as the high throughput necessary for volume production. These performance characteristics are critical for both launching new products and ongoing manufacturing monitoring. Bridging design and test to enhance yield management, Verigy’s Triage and YieldVision software tools capture failure data and perform yield analysis. This enables design-centric analysis and visualization on Verigy’s V93000 SOC test platform by integrating on-tester, real-time capture and analysis of electrical failures on complex SOC devices.

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Memory business models and device scaling are facing challenges due to high manufacturing costs, a low fab return-on-investment (ROI), a limited number of read and write cycles in Flash memories, and capacitor scaling limitations for dynamic random access memory (DRAM) cells. The cost for double patterning with immersion lithography and cost of ownership for next-generation lithography tools such as extreme ultraviolet (EUV) are increasing sharply.

Hence, emerging memories, based on new material and device concepts such as phase-change, magnetic, spintronics and resistive memories, are being developed. However, it is difficult for emerging memories to catch up to the density of conventional single-crystalline silicon memories because, fundamentally, the device pattern density depends on the minimum lithography feature size, not on materials. Further, material breakthroughs must be realized for these emerging memories to be successful before market introduction. Therefore, it is generally believed that the chance is slim for these emerging memories to penetrate majority memory markets in the near future.

To overcome these challenges to the memory business model and device scaling, low-cost, high-density memory cell stacking in three-dimensional (3D) ICs is promising. Unlike well-known 3D through-silicon vias (TSVs)—a package-level technology—the true 3D IC must be able to stack high-density, multi-memory layers sequentially on top of other device layers in a single chip at low cost using proven material and device technologies.

3D IC vs. 3D Package with TSV

3D TSV packaging is used for 3D image sensors and will be used for some memory device applications. Compared to printed circuit board (PCB) integration, TSVs can have short distance interconnects, leading to enhanced system performance. In addition, because they stack multiple chips, TSVs have excellent small form factors which are especially important for mobile devices. However, the integration level is limited to a few hundred interconnects per mm², which is far less than single-chip integration levels which require millions of interconnects per mm². Hence, TSVs have limited bandwidth, and their application is limited to the package domain. Furthermore, it is not obvious that TSVs can reduce the cost of memory devices and increase memory density.

The true 3D IC, or simply 3D IC, should have solutions for low processing cost, low die cost, unrestricted 3D interconnects with high bandwidth, and high-density memory cells. Therefore, 3D ICs can overcome Moore’s Law and extend the pace of memory scaling at low cost. The concept is shown in Figure 1.

Memory Applications for 3D ICs

In general, the memory cost per bit can be reduced through memory cell size shrinkage. However, memory cell shrinkage requires new tool investment and resource investment for new technology and material development. 3D IC architecture allows for the implementation of next-generation memory devices with currently available tools and technologies.

In particular, capacitor shrinking is the bottleneck of DRAM cell size reduction. Stacking the capacitors along with access transistors on top of memory logic is effective to introduce next-generation DRAM chips without tool and resource investments for next-generation capacitor development because the 3D IC architecture allows for the stacking of more memory cells in the vertical dimension for a given silicon substrate area. Likewise, Flash memory can be implemented in 3D ICs through stacking Flash cell arrays on top of logic on the
silicon substrate. Memory expansion is relatively easy for 3D ICs because memory stacking is a repeating process without significant redesign of the logic area.

Considerations for 3D IC Architecture
There are two crucial considerations for the 3D IC architecture for high-density memories. One is low manufacturing cost to minimize the cost per bit, and the other is to utilize proven technologies, tools and materials as much as possible to minimize fab investment, maximize ROI, reduce risks of new technology development and achieve fast time-to-market.

As process steps are added to implement memory cells in 3D ICs, the manufacturing cost rises. To minimize the cost per bit, it is very important to reduce the additional manufacturing cost for each memory layer. It is believed that the first memory layer won’t increase the total wafer processing cost because 3D ICs are formed through the stacking of functional blocks. For example, DRAM manufacturing has about 10 extra mask steps for memory cell implementation. The 3D IC process locates these 10 mask steps from the bottom silicon substrate to the top of the logic. Hence, the total mask steps with the first memory layer are about the same. An additional DRAM cell layer is designed to use about six additional masks, representing about a 15 percent processing cost increment, while memory density increases 100 percent per each additional memory layer in 3D. Considering the sharp increase of manufacturing cost with double patterning using immersion lithography and EUV, the 15 percent processing cost increment per memory layer with old generation tools is likely the most affordable method to continue memory scaling, and low cost can be achieved with 3D ICs.

3D ICs for Silicon Memories vs. Emerging Memories
To overcome problems with memories, there are many activities in the industry and academia to replace silicon memories with emerging memories. However, emerging memories have not yet been successful because compared to emerging memories, silicon has an accumulated manufacturing experience of several decades, silicon processing technologies and tools are well established, silicon memory devices are fundamentally stable, and silicon dioxide is reliable and easy to use. Recently, some emerging memories have successfully demonstrated 3D stacking capability. However, a fundamental issue with emerging memories is not the 3D processing technology, but the quality of new and sometimes unproven materials. Without breakthroughs in material quality, emerging memories will be unable to compete with silicon memories in high-density memory markets, but research on emerging memories will continue and will be necessary for the future of the semiconductor memory industry. However, the chance that emerging memories will replace silicon memories in the near future looks very slim. Therefore, it is desirable for 3D ICs to use reliable silicon memory technologies based on metal oxide semiconductor field-effect transistors (MOSFETs) and existing tools.

Memory Device Functions with 3D ICs
Since simple memory cells are stacked on top of logic with proven memory cell structures (i.e., “one transistor plus one capacitor” cell for DRAM and one transistor cell for Flash memory), good device characteristics and high reliability can be achieved. Basic memory cell device functions such as read/write/refresh of DRAM and program/erase are shown in Figure 2.

New 3D IC Manufacturing Model for Memories
The semiconductor industry needs to find a way to minimize the tool investment for high and fast ROI. Without high growth and high profits, the semiconductor industry will quickly mature similar to the auto and airline industries. Due to the steep decrease of the average selling price (ASP), revenue growth of the memory industry is being slowed while the required tool investment increases sharply, leading the memory business to change its business model.

Figure 3 shows a new memory business model which utilizes 3D IC processing at a new fab, while old generation fabs process logic for memory devices. Traditionally, a fab processes wafers for about eight weeks and transfers the finished wafers to assembly and test. Fab ownership cost has reached $4 billion and continues to rise every year, making ROI from fab investment extremely difficult. For example, a fab with a $4 billion investment needs to make a $10 billion profit over the next four years to compensate the depreciation of existing fab tools if the total depreciation of fab tools takes four years. And reserve cash for the next-generation fab investment might be $6 billion in the near future. To make a $10 billion profit over four years, a company which owns an advanced fab may have a 25 percent market share of the $40 billion memory market with 25 percent margins for four years. It is very difficult to do this, and only a few top-tier companies can survive the memory business.

3D ICs for memory applications have two functional parts. One is the logic on the bottom and the other is the memory cells on top. The processing time for logic with about 30 mask steps is about six weeks, and the processing time for a memory cell with about 10 masks takes about two weeks. Because memory logic does not use advanced feature sizes, it can be processed in established fabs, and high-density memory cells can be processed at new but small fabs. In other words, for two weeks of memory cell wafer processing with
Apache Design Solutions, the technology leader in power and noise solutions for chip-package-systems (CPS) convergence, announced that Sigma Designs, a leader in digital media processing system-on-chip (SOC) solutions for consumer electronics, adopted Apache’s register transfer level (RTL) to sign-off power and noise integrity products. PowerArtist-XP™ provides a complete RTL power optimization platform with fully integrated advanced analysis and automatic reduction. RedHawk™ enables full-chip dynamic power analysis from early-stage design to sign-off.

In September 2009, Apache acquired Sequence Design, expanding the company’s product offerings from the earliest stages of RTL design all the way to the physical sign-off level. Sigma Designs chose Apache to analyze power as early in the design flow as possible for maximum impact on cost control and chip power.

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ICsense is an IC design house with core competence in analog, mixed-signal and high-voltage IC design. The company offers best-in-class IC design services from consultancy and building block design up to complete turnkey application-specific IC (ASIC)/SOC solutions. The mission of ICsense is to be the number one long-term partner for innovative high-performance mixed-signal and high-voltage customer-specific IC developments. ICsense tackles these developments with a highly skilled and passionate engineering team, a structured IC design methodology, ISO 9001:2000 certified quality procedures, and close cooperation with its customers and partners.

The company offers customer-specific ASIC turnkey solutions, from idea to final product, including feasibility study, system definition and modeling, design, layout, prototyping, prototype testing, production test and assembly coordination. ICsense has key IC design experience in power management, high-voltage IC design, drivers, microelectromechanical systems (MEMS), sensor and actuator interfacing ICs, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), timing circuits and ultra-low-power design.

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Mentor Graphics is a world leader in electronic design automation (EDA) products, consulting services and award-winning support for electronics and semiconductor companies. Mentor offers solutions that meet the demand for short design cycle time, improved productivity and acceptable yield. Its solutions include tools for electronics system-level design and simulation, embedded hardware and software co-development, system and IC verification, IC physical design and verification, yield enhancement and testing of sub-65nm ICs. Mentor’s products include the Olympus-SOC place-and-route system; the Calibre physical verification suite; Calibre design-for-manufacturability (DFM) solutions for random, systematic and parametric issues affecting yield; and the comprehensive Tessel suite for production test, built-in self-test, failure diagnosis and accelerated yield learning.

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Mixel is a leading provider of mixed-signal IP, announced the availability of the first Mobile Industry Processor Interface (MIPI)/Mobile Display Digital Interface (MDDI) unified physical layer (PHY) IP solution. The MXL-PHY-MMU-RX3 combines a MIPI D-PHY compliant with revision 1.0 of the MIPI standard with an MDDI-PHY compliant with revision 1.2 of the MDDI standard.

Mixel is a leading provider of mixed-signal IP cores to the semiconductor and electronics industries. Mixel’s mixed-signal IP portfolio
Novocell Semiconductor announced the development of 2nTP™, a new multi-time programmable (MTP) technology that allows for the programming of its one-time programmable (OTP) technology. With the exception of foundry processes. These characteristics include high performance PHYs, serializer/deserializer (SerDes), transceivers, phase-locked loops (PLLs), delay-locked loops (DLLs) and analog building blocks, which are used in mobile applications such as MIPI, MDDI, networking and storage.

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MoSys, a leading supplier of high-density embedded memory and high data rate parallel and serial interface IP, announced the availability of its silicon-proven double data rate, third generation (DDR3) and DDR3/2 combo PHYs. MoSys’ fully integrated solution complies with the latest DDR PHY Interface (DFI) specification and provides the PHY interface between the controller logic and DDR3/2 DRAM devices. The DDR3/2 PHYs can achieve data rates up to 1600Mbps in a wirebond package and 2133Mbps in flip-chip packaging, making them well-suited for both high-performance and cost-sensitive designs.

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Sidense provides secure, very dense and reliable non-volatile OTP memory IP for use in standard-logic CMOS processes with no additional masks or process steps required and no impact on product yield. The Company’s innovative one-transistor (1T)-Fuse™ architecture provides the industry’s smallest footprint, most reliable and lowest power NVM IP solution. With over 40 patents granted or pending, Sidense OTP provides a field-programmable alternative solution to Flash, mask read-only memory (ROM) and eFuse in many OTP and Media Transfer Protocol (MTP) applications.

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Sofics is the leading on-chip electrostatic discharge (ESD) solutions and IP provider, well known for its TakeCharge specialty ESD solutions in low-voltage sub-micron and nano CMOS technology. Recently, Sofics announced a new portfolio called PowerQubic, which is comprised of ESD solutions with amazing breakthrough characteristics for high-voltage and power IC applications and processes. These characteristics include high ESD robustness (scalable 2kV-4kV-8kV); very low leakage (–nA at 25°C, ~100nA at 125°C); guaranteed latch-up immune with full current clamping above the high-voltage supply level and across the full temperature range; smallest silicon area footprint; lowest capacitance; tunable trigger and holding current and voltage (Vt1, It1, Vh, It2, Vt2); and cost-effective ESD protection reliability for supply pins as well as for input/output (I/O) interfaces, switches and large driver circuits.

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Virage Logic’s new ARC 601 32-bit microprocessor core offers the best-in-class combination of small size and low power with excellent performance. Designers can tailor the highly configurable ARC 601 to meet their specific application needs by excluding features that are not required, thereby reducing area, power consumption and cost. The ARC 601 runs at 532MHz (1.2 DMIPS/MHz), consuming just 13µW/MHz in 65nm process technology. At only 0.039mm², the ARC 601 will fit two and a half times into the size of a period (12-point font) at the end of a sentence. The processor is available today and has already been licensed to several of Virage Logic’s lead customers.

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Oracle provides industry-leading business solutions for the semiconductor industry based on best-of-breed applications; middleware; and open, standards-based technology. Oracle’s supply chain solution helps semiconductor companies achieve accurate consensus forecasts, optimized inventory leveling and postponement strategies, faster planning cycles and superior on-time delivery. While Oracle’s acquisitions have certainly added value to their comprehensive solution capabilities, few have recognized the continual innovation of new functionality which stems from their annual research and development (R&D) efforts, worth $3 billion annually. This fall Oracle will release a newly developed standalone product, Oracle Rapid Planning. The product will answer the “what if” questions that arise and will allow supply chain planners to react in minutes to rapidly changing conditions and exceptions in a semiconductor company’s complex, multi-tiered supply chain. Using an intuitive new user interface (UI) and an event-based, scalable, incremental planning engine, Oracle Rapid Planning enables a real-time planning paradigm providing capabilities to simulate the impact of events and use embedded analytics to gain predictive and actionable insight. Please contact Oracle to request a demo of the new Oracle Rapid Planning.

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Siemens is a semiconductor company with offices in Lubbock, Texas and Santa Clara, California. The company offers full turnkey 100 percent domestic content from RTL development to packaged and tested silicon. SiliconXpress maintains the necessary clearances required for customers’ trusted programs. With the exception of foundry services, all other IC services, including design, packaging and testing, are performed in-house.

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Identifying Optimal Non-volatile Semiconductor Memory for Use in RAID Systems

Barry Hoberman, Business Development, Crocus Technology
Steve Cliadakis, Business Development, Crocus Technology & Silicon Impact

Redundant array of inexpensive disk (RAID) systems increase server performance and protect against data loss by exploiting disk-level parallelism. Without RAID servers, there would essentially be no commercial Internet. Because they hold mission-critical data and must provide fault-tolerant storage, enterprise customers cannot tolerate any potential for RAID server data loss in a world of less-than-perfect electrical power sources. Consequently, RAID system designers have tried using many non-volatile semiconductor memories, including NAND Flash, non-volatile static random access memory (NVSRAM), ferroelectric RAM (FeRAM or FRAM) and magnetoresistive RAM (MRAM), to retain data in the event of a power failure. Of these, MRAM comes closest to the ideal memory for RAID system server design.

The commercial behemoth known as the World Wide Web sits layered on an intricate, distributed data network called the Internet. System architects build and extend the Internet’s very foundation using storage blocks called hard disk drives (HDDs). Shelves full of HDDs organized into RAID systems inhabit countless racks in worldwide data centers. The improved performance and fault tolerance of RAID systems explain their universal acceptance as the local and networked storage medium of choice for all types of Internet servers, other on-line transaction processing (OLTP) servers, and many other server types installed in large and small data centers worldwide. According to estimates and forecasts, several million of these servers ship each year.

RAID systems use sophisticated, fault-tolerant methods of data storage, including data mirroring and striping, to distribute data across multiple drives and thus protect data against loss. These methods make automated recovery possible when an individual HDD fails. Real-time data recovery, possible with more advanced hardware RAID systems, ensures that important and mission-critical data remains safe even after catastrophic hardware failure. Although a RAID system’s disk drives provide much of the non-volatile data storage needed to provide fault-tolerant operation and data recovery ability, there is a real need for non-volatile semiconductor memory within the design of the RAID controller. Without non-volatile chip memory, a RAID system cannot protect data against certain types of failures such as power loss.

Figure 1 shows a block diagram of a RAID system. The RAID server’s heart is the RAID control processor, which manages the attached drive array through a bank of industry-standard serial attached SCSI (SAS) and serial ATA (SATA) drive interfaces. Although largely based on HDDs, RAID systems increasingly include one or more solid-state drives (SSDs), which themselves are based on arrays of NAND Flash semiconductor memories. SSDs provide roughly 10x faster write performance and 100x faster read performance than HDDs, but they cost substantially more per gigabyte (GB) of storage. Hybrid RAID systems that combine HDD and SSD storage currently offer the best available mix of performance and capacity. Note that Figure 1 shows a superset of all possible methods used to provide non-volatile storage in the server (shown as colored boxes). Practical RAID designs use some but not all of these methods.

Figure 1. Block Diagram of a RAID Server
The RAID control processor currently requires a mix of semiconductor memory, including DRAM and non-volatile semiconductor memory. Local non-volatile memory usually serves as a repository for the hardware RAID server’s firmware and as non-volatile storage of configuration data and of a journal/transaction/error log file. The right side of Figure 1 shows a large box labeled “Primary RAID Memory Cache.” This cache speeds disk write transactions from the host server’s perspective. The RAID controller can quickly stash write transactions in fast memory cache and then signal transaction completion to the host. Then, the RAID controller moves the transaction data from the primary cache into the disk array, which is a relatively slow process compared to saving the transaction in the cache.

A large DRAM bank serves as the primary cache in most RAID servers because DRAM currently provides the best available combination of fast write time and low cost/bit. Low per-bit cost is important because RAID memory caches are sometimes as large as 32GB. Today, this DRAM is most likely to be double data rate, second generation synchronous dynamic random access memory (DDR2 SDRAM), which will quickly transition to DDR3 SDRAM this year as sales volumes and semiconductor memory economics start to favor DDR3 SDRAM over DDR2.

However, DRAM has a severe liability when used as RAID memory cache: DRAM provides only volatile storage. If power is lost, so is the data stored in the DRAM. Because RAID systems hold mission-critical data and must provide fault-tolerant storage, enterprise customers cannot tolerate this potential for data loss in a world of less-than-perfect electrical power sources. Consequently, RAID designers employ one of several methods to add non-volatile storage to DRAM-based primary caches.

The first such method is to simply add a battery and power controller to maintain power to the primary cache when power mains fail. However, most battery systems used in RAID applications are rated for no more than 72 hours of unpowered operation. After that, data may be lost. Batteries also require maintenance. RAID back-up batteries should be replaced annually, which is both an extra expense and a potentially serious operational problem. It’s not uncommon for data center managers to be blissfully unaware that their RAID servers contain deeply embedded batteries. Consequently, many RAID back-up batteries are not serviced regularly, and mission-critical data is at risk.

Figure 1 shows an alternative design approach—adding NAND Flash memories to the primary cache—which also provides non-volatile storage for the RAID system’s primary cache. When the RAID control processor detects a loss of main power, an inexpensive back-up control processor in the primary cache independently copies the contents of the cache’s DRAM to the NAND Flash array. NAND Flash is generally rated to safely hold the data for 10 years without power. Battery power is only required for a short period while the data is copied from DRAM to NAND Flash. Some designs dispense with the battery and the associated maintenance requirements and instead use low-maintenance ultra capacitors, which provide the needed power for the short back-up interval. Using Flash as a back-up memory layer in this configuration adds the cost of the Flash memory itself, as well as the supporting back-up circuitry and hardware, to the RAID system.

Two key characteristics prevent NAND Flash from being used as the sole memory in primary RAID caches. First, NAND Flash devices have relatively long write latencies due to their long erase-write cycles. Second, NAND Flash devices deteriorate in direct proportion to the number of erase-write cycles they endure. Most NAND Flash devices are rated for only 100,000 or so erase-write cycles before the serious onset of memory cell failures. Wear-leveling techniques remediate NAND Flash wearout failures in SSD applications, but these techniques are too slow to apply to a primary RAID cache, which requires data throughput rates that are orders of magnitude faster. These two traits greatly reduce the attractiveness of NAND Flash for direct primary cache storage. For these reasons, NAND Flash can serve as a DRAM back-up in the primary RAID cache but cannot serve as the primary cache’s main memory alone. There’s a significant opportunity to replace DRAM in the primary RAID cache if a cost-competitive, non-volatile semiconductor memory with DRAM’s write speed and without NAND Flash’s write endurance problem becomes available.

Beyond the primary RAID memory cache, two other places in the RAID server block diagram require non-volatile memory—for firmware storage and for the journal/transaction/error log file. Use of non-volatile memory such as read-only memory (ROM), electronically programmable ROM (EPROM) and NOR Flash for firmware storage is pervasive in most embedded systems, including RAID servers. However, the log file is unique to storage applications.

Journaling file systems employ techniques from transaction processing database systems to maintain the structural consistency of the data stored in the RAID array by logging atomic disk input/output (I/O) transactions. Should a failure occur such as the loss of a drive in the disk array, replaying the transaction log from the last file system checkpoint restores the RAID system’s state. Depending on the checkpoint frequency, the journal/transaction/error log file need not be nearly as large as the primary RAID memory cache. A few megabytes of storage are generally sufficient for both the journal/transaction/error log file and the RAID system’s configuration data. For obvious reasons, the memory that holds these files must be non-volatile.

Several semiconductor memory technologies vie for this socket: NVSRAM pairs a six-transistor (6T) static RAM cell with a silicon-oxide-nitride-oxide-silicon (SONOS) electrically erasable programmable ROM (EEPROM) cell, replicating the SDRAM/NAND Flash pairing previously described but at the cell level. The result is a fast SRAM array that can be backed up in one write cycle. NVSRAM is currently the technology of choice for the non-volatile memory in RAID systems (excluding the primary memory cache). However, the NVSRAM memory cell is more than twice as large as a 6T SRAM cell, which itself is relatively large compared to DRAM or NAND Flash memory. Consequently, NVSRAM storage is relatively expensive on a cost/bit basis and will likely stay that way relative to other memory technologies.

FRAM inserts a ferroelectric material, typically lead zirconate titanate (PZT), into the semiconductor processing flow. The ferroelectric material creates a bistable bit storage element that operates at the molecular level. An electric field sets the physical
ASIA

>40% – Percentage growth of set-top box (STB) shipments in Asia in 2009. The European market saw unit shipments fall 11% in 2009. – In-Stat

32% – Year-over-year (YoY) growth of the Asia-Pacific (excluding Japan) PC market in Q4 2009, with portable PCs as the key driver. – International Data Corporation (IDC)

20% – Percentage of Japanese engineers that would “like to change” employers “within a few years” or sooner. This may be due to Japan’s struggle for relevance in a technology world that is shifting resources and manufacturing to China. – 2009 EE Times Global Salary & Opinion Survey

$85 billion – Estimated revenue China’s IC market will generate by 2011. Domestic chip production is expected to reach $8.2 billion. – iSuppli, IC Insights and China Semiconductor Industry Association (CSIA)

10.7% – YoY growth of China’s gross domestic product (GDP) in Q4 2009. – Chinese Government

35% – China’s projected share of the global chip market in 2013. – Semiconductor Equipment and Materials International (SEMI)

3 million – Predicted number of e-readers sold in China in 2010, accounting for 20% of the global e-reader market. This number is a massive jump from 800,000 units sold in 2009. – DisplaySearch

$4.1 billion – Estimated revenue generated by the portable electro-medical device market in China in 2011. The growth of this market is due to the government’s medical reform, citizens’ concern about healthcare and the devices’ unique features. – EE Times Asia Article, “Portable Medical Electronics See Big Market in China”

10% to 15% – Expected percentage decline of electronic exports in the Philippines in 2009. – Semiconductor and Electronics Industries in the Philippines Inc. (SEIPI)

$50 million – Amount of capital the South Korean government will inject into local semiconductor manufacturing equipment companies over the next three years. – South Korean Government

6 – Number of Taiwanese semiconductor companies ranked as top 25 fabless IC suppliers in 2009. The companies are MediaTek, Novatek Microelectronics, Himax Technologies, Realtek Semiconductor, MStar Semiconductor and Richtek Technology. – IC Insights

3.1% – Expected growth of Taiwan’s IC design production value in 2009, further expanding by 16.4% in 2010. – RNCOS

0.08% – Anticipated compound annual growth rate (CAGR) of total telecom spending in Sri Lanka during 2008 to 2015, reaching $593 million. – Frost & Sullivan

2.4% – Projected CAGR of total telecom spending in Bangladesh during 2008 to 2015, reaching $2,060 million. The growth in spending in this region will be driven by the untapped rural market. – Frost & Sullivan

INDIA

>$50 billion – Estimated export revenue generated by business process outsourcing (BPO) and information technology (IT) companies in India in 2009. This figure is predicted to grow 13% to 15% in 2010, reaching $56 to $57 billion. – National Association of Software and Service Companies (NASSCOM)

$22 billion – Amount that will be spent by India on IT services in 2009. – IDC

130 million – Number of handset units India shipped in 2009. This figure is expected to escalate to 150 million in 2010. – mydigitalfc.com Article, “Handset Market Attracting More Players”

$20 billion – Revenue generated from the domestic production of electronics in India in Q4 2009, growing 16% YoY. – India Semiconductor Association (ISA)

2.2% – Anticipated CAGR of total telecom spending in India during 2008 to 2015, reaching $25,129 million. The capital expenditures will be driven by 3G operations that are expected to start in the next one to two years and the thrust on broadband and carrier services by current larger operators. – Frost & Sullivan
100 million – Estimated number of broadband subscribers in India by 2012. TV, if used as an end-user device, will be the main driver to increase broadband penetration from the present seven million subscribers in the region. – UT Starcom India

3 million – Forecasted number of car units in India by 2016. – Society of Indian Automobile Manufacturers

20% – Forecasted percentage of leading cloud aggregators in the market that India-centric IT companies could potentially represent through cloud service offerings. – Gartner

$4.4 billion – Value of electronic exports in India in 2009, representing 21% of domestic production. Electronic exports in India grew 19.5% YoY in Q4 2009. – ISA

6.0% to 6.5% – Expected growth of India’s GDP in Q4 2009, a decrease from 7.9% growth in Q3 2009. – Indian Government

58% – Percentage of venture capitalists that anticipate an increase in the number of India-based investments in 2010, while 70% anticipate growth in China-based investments. – National Venture Capital Association’s (NVCA) Venture View 2010 Survey

21% – Percentage decrease of the European electronic components market’s billings compared to 2008. – International Distribution of Electronics Association (IDEA)

-1.6% – Estimated CAGR of total telecom spending in Saudi Arabia during 2008 to 2015, declining to $5,875 million. – Frost & Sullivan

-0.02% – Estimated CAGR of total telecom spending in United Arab Emirates (UAE) during 2008 to 2015, slightly declining to $1,262 million. – Frost & Sullivan

$1.6 billion – Value of venture capital investment in clean technology by European and Israeli companies in 2009, marking the second highest funding year. Total investment was down 12% from 2008 but up 30% from 2007. There was a record 214 deals completed, slightly surpassing the 212 deals completed in 2008. – Cleantech Group

$49.5 million – Amount of funding raised by four Israeli semiconductor companies in 2009. – GSA

$291 million – Amount of clean technology funding raised in 61 U.K. deals in 2009, registering a dollar amount increase from 2008. Norway raised $234 million in 12 deals, while Germany raised $207 million in 17 deals. – Cleantech Group

46% – Percentage of European engineers that rated photovoltaic (PV) technology as a promising area in today’s industry. North American, Indian and Chinese engineers followed with 45%, 21% and 11%, respectively. The response from Chinese engineers was surprising since the country is the world’s leading producer and exporter of PV cells. – 2009 EE Times Global Salary & Opinion Survey

15.5% – Projected CAGR of the number of mobile subscribers in Nigeria during 2010 to 2012. This growth is due to the country’s rapidly improving mobile infrastructure and intense competition among mobile operators. – RNCOS

THE AMERICAS

$863.3 million – Value of orders posted by North America-based manufacturers of semiconductor equipment in December 2009. – SEMI

$3.8 billion – Amount raised from 32 funds by U.S. venture capital firms in Q4 2009. – Thomson Reuters and NVCA

30% – Percentage of automotive models sold in the U.S. in 2009 with installed telematic systems, making it the world’s leading market for telematics last year. In comparison, the next two biggest telematics regions, Germany and Italy, have only 20% model availability of installed telematics systems. U.S.’ leadership is due to General Motors which pioneered installed telematics. – iSuppli

2.5% – Growth of U.S. productivity, in per hour terms, in 2009. – The Conference Board

262 – Number of venture-backed acquisitions in the U.S. in 2009, declining 31% from 2007. – NVCA

28.3 million – Expected number of U.S. consumers that will have Internet access in their cars by 2016, a significant increase from 520,000 consumers in 2009. – iSuppli

0.3% – Expected growth of the U.S. consumer electronics industry in 2010, reaching sales of $165.3 billion. This increase will be driven by the growing popularity of smartphones and netbooks. – Consumer Electronics Association (CEA)

85% – Percentage of U.S. households that are willing to pay $80 to $100 for cost-saving equipment if they are guaranteed to save 10% to 30% off their monthly electricity bill. – Parks Associates

20.7 million – Number of PC units shipped in the U.S. in Q4 2009, increasing 24% YoY. This unit growth was led by a holiday season featuring price cuts of unprecedented duration. – IDC

$95.8 billion – Amount of funding raised by 331 private equity funds in the U.S. in 2009, down 68% from $299.9 billion raised by 508 funds in 2008. – Dow Jones

10 million – Expected number of liquid crystal display (LCD) TV unit shipments in Brazil in 2010. – DisplaySearch
A universal memory fulfills every system architect’s needs: a single memory that is high-speed, high-density and non-volatile and has unlimited endurance with long-term data retention. Universal memory has been the elusive prize since bubble and charge-coupled device (CCD) memories were thought to be the answer in the late 1970s. Though these and other technologies have come and gone, there is a new generation of memories looking to claim the prize; but are these technologies any closer to meeting the ever-increasing performance and cost requirements of the electronics industry’s demands?

Roughly speaking, computer systems partition memory into three primary blocks: cache memory tightly coupled to the central processing unit (CPU), main memory managed by a memory controller and code/data memory managed by an input/output (I/O) controller. Currently, cache and main memory are thought of as being solid-state, while the code/data memory is a form of disk or disk array, historically rotating but moving toward solid-state. Cache memory is usually fast, small, integrated into the CPU and implemented with static random access memory (SRAM). Main memory is larger and slower than cache and is usually implemented with dynamic random access memory (DRAM). Both of these technologies are volatile, losing data when power is removed.

Figure 1 demonstrates memory requirements within a generic system hierarchy. In today’s systems, the working memory is fast but usually volatile. In some cases, these memories or portions of them are made non-volatile by adding battery back-up in the form of uninterruptable power supplies or dedicated battery subsystems. System architects use code/data storage for information that must be retained when power is removed while requiring much higher densities. Code/data storage memory is non-volatile, typically implemented as a rotating disk or solid-state Flash, and may have additional battery-backed RAM. In all cases, compromises are made to support the specific function.

Rotating disk drives deliver the densities and non-volatility but with much slower performance than SRAMs and DRAMs. New solid-state drives (SSDs) using NAND Flash exceed rotating media’s performance but suffer from reliability concerns. SSDs may use other semiconductor memories such as SRAM or DRAM to improve performance and reliability. High-performance battery-backed DRAM caches provide additional throughput and data integrity improvements to storage systems.

**Figure 1. Memory System Architecture**

Block diagram representation of a generic computer system hierarchy.

Douglas Mitchell, Vice President, Sales and Marketing, Everspin Technologies

**High-performance, Non-volatile Memories: And the Winner is...**
SRAM, DRAM and Flash have become industry-standard solutions to this wide range of memory requirements. SRAM and DRAM are both volatile, losing data when power is removed. SRAM can have synchronous, wide-word interfaces for very fast access or easier-to-use asynchronous interfaces for general-purpose applications. Batteries are used to make them "non-volatile," but these memories still carry reliability, wear-out and environmental limitations. DRAM is available with various high-performance interfaces but requires continuous power to operate. Flash memory and its technological cousin electrically erasable programmable read-only memory (EEPROM) have made great strides to increase density while reducing costs, but as these attributes improve, data retention and endurance suffer. Slow write speeds continue to be Flash’s Achilles heel. Is there a technology on the horizon capable of becoming the universal memory?

Four technologies currently in development have the potential of fulfilling many of the characteristics required by a universal memory: phase-change random access memory (PRAM), resistive random access memory (RRAM), ferroelectric random access memory (FeRAM) and magnetoresistive random access memory (MRAM). Each attempts to implement a combination of process and design technologies where data is written directly to the memory cell to achieve high speed, high density and low cost while incorporating non-volatility with robust endurance and retention characteristics.

A detailed comparison of performance features for each of these technologies is appropriate for later discussion. This analysis is intended to briefly overview the characteristics of each technology by highlighting the promise for each in the marketplace and where the technologies best serve a system solution.

PRAM is based on the ability to switch a chalcogenide material (generally an alloy of germanium, antimony and tellurium) from a crystalline state to an amorphous state and back by applying various levels of current to the storage element, resulting in higher or lower heat in the storage element. The storage element's data state is sensed by measuring the resistance of the element after it has stabilized into its crystalline, low-resistance or amorphous, high-resistance state. PRAM has the characteristics of being bit-level programmable, reasonably fast to read and write, and has endurance superior to current Flash products. It does, however, suffer from sensitivity to high temperatures, which make it difficult to use in harsh environments and may require programming after being assembled into systems using high-temperature solder processes. Although PRAM development has been active since the 1970s, recent developments indicate that commercial products over 100Mb in density may be available soon, but with performance compromises that limit endurance cycling to one million cycles and write cycle times to slower than 100ns.

RRAM is based on the ability to switch the characteristics of certain materials by applying current pulses that change the crystalline structure, resulting in a change in resistance. A number of alloys are being studied that exhibit these characteristics. This technology holds the promise of a very small cell size built on sub-30nm complementary metal-oxide semiconductor (CMOS) processes, resulting in large memory densities. The non-volatile memory element would rely on perovskite-oxide thin-film materials, advanced photolithography processes and diode switching (instead of transistor switching) to create very small memory elements. Progress has been made on developing memory arrays using these techniques with the promise of achieving high densities and faster writes than Flash. Endurance and speed performance, however, are not yet capable of meeting mainstream memory requirements. Current solutions are demonstrating write cycle times in the microsecond range with million-cycle endurance.

FeRAM is built with a cell structure similar to DRAM which uses a one-transistor and one-capacitor storage element to retain charge. FeRAM replaces the DRAM charge storage capacitor dielectric with a ferroelectric material, typically lead zirconium titanate (PZT), strontium bismuth tantalate (SBT) or bismuth lanthanum titanate (BLT). The crystalline ferroelectric material will orient its electric dipole in one direction or the other based on the application of an electric field to the capacitor plates. After orientation to a "one" or "zero" state, the bit can be read by applying a voltage to the cell and sensing whether a pulse is generated if the cell is being switched to its opposite state. If not, then it was already in the sensed state, say a 0; if so, a pulse is created by the dipole switching, indicating a 1. If the cell did switch states, it must be restored to its original state before further operation. Low-density FeRAM has been in commercial production for many years but has suffered from the inability to scale to densities higher than 4Mb. It has moderate speed and limited read/write endurance, although far better than Flash. There is little indication that FeRAM has enough industry support to achieve significant improvements required to break through these limitations to allow it to participate in high-volume applications.

MRAM has emerged as the most promising of these memory technologies for approaching the needs of many applications in the system hierarchy. Currently, commercial MRAM products are shipping into the marketplace, establishing the technology’s viability as a production technology capable of meeting demanding performance requirements. The MRAM memory cell stores data using a magnetic tunnel junction (MTJ), a small device having two ferromagnetic layers separated by a thin dielectric layer. It has two stable magnetic states, one with the layers polarized in the same direction and the other with its magnetization directions in the opposite direction or anti-parallel. The resistance of the MTJ is low if they are parallel and high if they are anti-parallel. Reading an MRAM bit is accomplished by sensing the resistance of a small current passed through the MTJ.

There are two major types of MRAM that are being commercially pursued: toggle MRAM and spin-torque MRAM. Each uses a different technique to write the memory bits. The write operation for a toggle MRAM is accomplished by passing currents through adjacent copper lines to generate the specific magnetic field pulses needed to reverse the magnetization state. Only bits at the cross-point of two write lines will receive the correct pulses to be written. Other bits in the array do not see the appropriate pulses and will not change state. This write scheme is non-destructive and allows random access of any address in the array. High volumes of toggle MRAM are shipping today into demanding applications such as storage, industrial automation and energy management systems.

In spin-torque MRAM, the magnetic state is switched by using a magnetic field from current passed directly through the MTJ, rather than the field generated from electrically isolated current lines. The spin-torque effect switches the device to the parallel state when the current is passed in one direction and to the anti-parallel state when the current is reversed. This type of switching eliminates one of the current carrying lines, enabling a more dense architecture with a cell size comparable to DRAM. While toggle MRAM will continue to scale to higher densities, spin-torque MRAM provides the promise of achieving high speeds, high densities and low costs.
With a one-of-a-kind memory business model, Phison Electronics met with great success in 2009 and optimistically looks forward to having another thriving year. In my interview with Khein-Seng Pua, chairman of Phison Electronics, we discussed how its customers benefit from the company’s unique expertise; what markets will fuel the growth of NAND Flash; the increasing need for data security solutions; and much more.

— Jodi Shelton, President, GSA

**Q:** A very rare feat, Phison Electronics experienced continuous sequential revenue growth throughout 2009. And with strong orders coming in, the company is reportedly on track to have a prosperous Q1 2010. What do you attribute Phison’s success to?

**A:** Phison achieved record revenue in 2009, and we are optimistic about Q1 2010 as the company continues to prosper with the growing momentum of NAND Flash. Phison’s success is attributed to the uniqueness of the company; there is no other company in the industry with our business model. We are not simply a module house or fabless company—we act as both. Phison is a NAND Flash solution provider that supports brand name companies. With our advanced controller technologies and system integration expertise, we provide competitive products to our customers that allow them to focus on managing their brands and not worry about technical issues. Our customers view Phison as their research and development (R&D) center, manufacturing site as well as industrial designer. Moreover, Phison customers greatly benefit from our partnership with upstream Flash vendors; they never have to worry about NAND Flash supply shortages. A stable supply is guaranteed in this dynamic industry.

**Q:** Phison recently announced that it will make an advance payment of $50 million for NAND Flash chips, conveying that the company anticipates growth in the NAND industry. What markets do you see driving the growth in the NAND industry. What impact will this product have on the NAND Flash sector?

**A:** Flash vendors are working on alternatives to Flash such as phase-change memory (PCM), resistive random access memory (RRAM) and 3D memory to ensure that cost-effective non-volatile memory (NVM) is available in the future. In other words, they are trying to keep up with Moore’s Law. Other emerging memory technologies such as magnetoresistive RAM (MRAM) and ferroelectric RAM (FeRAM) have their niche in aviation, automotive and medical. These markets are less cost sensitive and are therefore not addressable by NAND Flash.

It is not clear which one of these alternatives will end up replacing Flash. NAND players are interested in technologies that provide high capacity and high performance at low cost and can compete with incumbent NAND Flash technology. In the next few years, NAND Flash will still be the most cost-effective NVM in the market. As a NAND Flash solution provider, Phison will support any kind of NVM as long as the chip is compatible with NAND Flash in terms of cost and performance.

**Q:** As I discussed earlier, NAND Flash is a fast-growing market. In the past five years, the NAND Flash market grew at a compound annual growth rate (CAGR) of 16 percent. We expect this growth to continue at the same speed in coming years due to the emergence of portable devices. We believe this market is still young, and there will be an increasing number of portable device applications surfacing in the future. Currently, 70 percent of NAND chips are consumed in consumer markets (e.g., mobile phones, digital still cameras and MP3 players), and volume is still growing. We see NAND adoption in systems picking up as well. Solid-state drives (SSDs) and embedded memory in mobile phones are the killer applications today.

**Q:** Phison has remained successful primarily as a supplier of NAND Flash solutions; however, are there other memory technologies that the company is eager to explore?

**A:** Flash vendors are working on alternatives to Flash such as phase-change memory (PCM), resistive random access memory (RRAM) and 3D memory to ensure that cost-effective non-volatile memory (NVM) is available in the future. In other words, they are trying to keep up with Moore’s Law. Other emerging memory technologies such as magnetoresistive RAM (MRAM) and ferroelectric RAM (FeRAM) have their niche in aviation, automotive and medical. These markets are less cost sensitive and are therefore not addressable by NAND Flash.

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**Q:** Apple recently unveiled its highly anticipated iPad, which relies heavily on NAND Flash. What impact will this product have on the NAND Flash sector?

**A:** Apple uses NAND Flash in all its products, making a great impact on the NAND Flash industry in terms of capacity and pricing. Apple certainly knows that NAND Flash provides better performance than heavy, power-hungry hard drives. It is very exciting to see Apple introduce new, revolutionary products each year and lead the trend in NAND Flash application. There is no question that there will be more electronic devices that follow suit and join the NAND technology bandwagon.

**Q:** The development of multi-bit-per-cell technologies, such as three-bit-per-cell (3bpc) and four-bit-per-cell (4bpc), has increased due to the technical challenges associated with process node migration and the surplus/declining pricing in the NAND Flash market. How long do you believe it will take to commercialize 3bpc/4bpc in Flash drives, memory cards, etc.?

**A:** It is already commercialized. Our controllers have been ready for 3bpc since 2008, and we are already using 3bpc chips in cards and Universal Serial Bus (USB) Flash drives. Phison’s controllers are of the very few that can manage 3bpc chips. Other NAND Flash vendors and controller makers are lagging in the 3bps race. Eventually, everyone will be able to provide the same solution,
Q: As Europe’s chip industry strives to achieve profitability, many European companies are implementing fab-lite models, consolidating and exiting the memory sector. As a Europe-based memory integrated device manufacturer (IDM), what has given Numonyx the rare competitive edge to remain successful in the devastated memory market?

A: Numonyx’s competitive edge is due to the company’s strong, unwavering market and technology leadership in today’s memory industry. We are currently one of the top non-volatile memory (NVM) companies in the world and the number one supplier of NOR solutions for wireless and embedded applications. Our NOR market share has experienced remarkable growth, increasing 4 percent quarter-over-quarter (QoQ) in Q3 2009, while the number two supplier’s share decreased 6 percent QoQ. In NOR’s two focused segments, wireless and embedded, Numonyx is currently the number one and number two leader, respectively.

Q: In 2009, various analysts proclaimed the memory business model broken and advised memory companies to consolidate. However, in Q3 2009, the memory sector saw companies such as Samsung Electronics and Hynix Semiconductor report double digit growth. Do you see this positive trend continuing, or is consolidation still critical? As a company that was created by two semiconductor powerhouse, Intel and STMicroelectronics, how do you feel this combination of key memory technologies has benefited Numonyx’s customers?

A: I would expect that the impressive financials of Samsung Electronics and Hynix Semiconductor are a result of the economy slowly recovering and the recent widespread consolidation. Numonyx experienced double-digit QoQ growth as well in Q3 2009, so we’re quite pleased with our results. With that said, I certainly believe that further consolidation within the industry is still needed.

When customers select memory suppliers in today’s industry, they are drawn to companies that deliver multiple technologies and invest in revolutionary solutions that will provide them value in the future. Through the combination of Intel’s and STMicroelectronics’ memory businesses, Numonyx is able to provide customers both of these benefits. The company offers customers a one-stop shop for all their memory solutions (i.e., NOR, NAND, random access memory (RAM) and phase-change memory (PCM)). Furthermore, the teaming of two prominent semiconductor leaders gives Numonyx customers confidence in the supply and product longevity of these technologies.

Regarding investment in innovation, Numonyx has put remarkable effort into the research and development of PCM, a breakthrough technology that promises to deliver solutions to many of the challenges facing the memory industry today. The merging of Intel’s and STMicroelectronics’ PCM development teams gives Numonyx the scale to significantly increase investment in PCM technology and bring it to the marketplace faster.

Q: Intel and Numonyx have aggressively pursued the development of PCM, a technology that fuses the speed of dynamic RAM (DRAM) with the non-volatility of Flash memory. With the cutting-edge capabilities and recent breakthroughs of PCM, many in the industry believe that it will replace Flash in future years. Do you foresee PCM being a “Flash killer,” and what impact will it have on the other established memory technologies? What efforts has Numonyx made to speed the adoption of PCM in the marketplace?

A: I don’t believe PCM technology is necessarily a “Flash killer,” as NOR Flash and NAND Flash both have a long lifetime ahead of them and are used in many applications. However, PCM does combine the greatest attributes of DRAM, NAND and NOR, enabling more capabilities on a single chip. PCM’s high-speed memory and its ability to erase the technology before writing it are certainly similar to DRAM, while its non-volatility parallels NAND and NOR. However, PCM cannot be directly substituted for DRAM, NAND or NOR technology, though it may attract a portion of their business. I strongly believe NAND and NOR customers will see and take advantage of this breakthrough technology’s value, helping it grow into a potential multi-billion dollar business. Consequently, there is a lot of market development work involved to ramp PCM technology. We believe there are new applications primary to the computing market that PCM technology has the ability to develop, and we are currently focusing our efforts on this.

We have two different efforts underway to successfully introduce

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EDWARD DOLLER
Vice President & Chief Technology Officer, Numonyx B.V.
Overcoming DRAM Scaling Challenges: Floating-body Memory Technologies, a Leading Contender for High-density and Embedded Memory Applications

Dr. Pierre C. Fazan, Chairman and Chief Technology Officer, Innovative Silicon S.A.

Scaling the conventional 1-transistor/1-capacitor (1T/1C) dynamic random access memory (DRAM) bit cell or the traditional 6-transistor (6T) static random access memory (SRAM) bit cell below the 40nm node dimension represents a serious technical challenge. In the area of DRAM bit cell scaling, contacts, device aspect ratios and capacitor materials are all approaching manufacturing limits. For SRAM bit cell scaling, variability and leakage issues impose severe constraints and may limit 6T historical cell scaling. Recently, new concepts have been proposed to address these scaling and performance limitations. Among them, the capacitor-less or floating-body (FB) memory cell is one of the leading contenders to replace DRAM and SRAM memories for embedded and standalone applications. This new technology is simple, uses only conventional materials and is therefore fully compatible with CMOS processes. Following the introduction of a technology exploiting a bipolar junction transistor (BJT) operation and its recent evolution toward three-dimensional (3D) devices and low-voltage operation, capacitor-less RAM cells are now well suited to replace standalone DRAM cells in sub-45nm memories.

History
Capacitor-less RAM technologies have significantly evolved over the years. The first attempt at exploiting a single MOS transistor to store information was made by Sasaki et al. of Fujitsu in 1978. They integrated a P-channel metal oxide semiconductor (PMOS) transistor with silicon-on-sapphire (SOS). By exploiting the FB effect of a single N-channel MOS (NMOS) silicon-on-insulator (SOI) transistor, a simpler and denser structure was proposed by Tack et al. of IMEC in 1990. The device operations described by these researchers were, however, incompatible with selective read/write operations and memory array implementation. That explains why the technical developments in this area stopped after these two first attempts. In 2001, Okhonin et al. of Innovative Silicon demonstrated that by properly pulsing the device gate and drain, a selective write/read operation was possible. This opened the door to memory array implementation. This successful array-compatible operation was also mentioned in 2002 by Ohsawa et al. of Toshiba. As illustrated in Figure 1, by exploiting a BJT operation, Okhonin et al. developed a technology exhibiting a higher signal-to-noise ratio, a longer retention time, a better scaling ability and full compatibility with future fully depleted (FD) 3D devices. The operating principle allows capacitor-less RAM cells to replace not only embedded DRAMs and embedded SRAMs, but also standalone DRAMs. This drastically increases the market opportunities for such a technology.

Figure 1. BJT FB Memory Exploiting a BJT Operation vs. Regular FB Memory Read Current and Retention Time

FB/Capacitor-less RAM Cells for Embedded Memory Applications
As previously mentioned, the FB/capacitor-less RAM bit cell and operating principle can be used to build embedded memories to replace embedded SRAM or embedded DRAM memories. Figure 2 shows the various bit cell layout possibilities for planar transistor structures. Embedded memories allow for the integration of cells having a 25F² to 45F² area (F being the minimum feature size of the technology). The cell area depends on the layout details. The cell becomes smaller when adjacent cells share source and drain terminals, and the cell becomes larger when one or two of the source and drain terminals of adjacent cells are separated.
Figure 2. FB Memory – Various Bit Cell Layout

- Embedded: 25F²
- Standalone: 4F²
- Embedded: 35F²
- Standalone: 6F²
- Embedded: 45F²
- Standalone: 8F²

Figure 3 illustrates a 4Mbit embedded FB memory block used as a cache SRAM replacement. It was developed for a 45nm high-performance logic process on SOI wafers. Read and write latencies of 2ns and 4ns, respectively, have been demonstrated. The memory density including array and periphery is more than three times the density of conventional embedded SRAM. Typical device retention times of 100ms have been achieved as shown in Figure 4.

Figure 3. 4Mbit Embedded FB Memory Macro

Figure 4. Typical Embedded FB Memory Device Retention Time

FB Memory as a Standalone DRAM Replacement

The FB memory/capacitor-less RAM bit cell and operating principle can also be used as a standalone memory replacement. Cell sizes of 4F² to 8F² are possible as illustrated in Figure 2. Here again, the cell area depends on the layout details. Figure 5 shows a scanning electron microscopy (SEM) image of a 6F² cell implemented in a 50nm DRAM technology. As can be seen in the picture, two adjacent cells share a common bit line or drain contact and have separated source nodes. Word lines and source lines run parallel to each other while bit lines are orthogonal. Such memory cells integrated with a DRAM process exhibit a typical retention time of a few seconds as shown in Figure 6.

Figure 5. 6F² Standalone FB Memory Bit Cell Cross Section

Figure 6. Typical Standalone FB Memory Device Retention Time

Scaling, Roadmap and Challenges

At 40nm and below, excessive device leakage resulting from aggressive device scaling severely affects both standby power and retention for DRAM and SRAM technologies. This has prompted 3D device structures to enter the various standalone memory technology roadmaps. These 3D structures also provide a benefit to FB memory cells and enable source and drain doping profile engineering to control and improve cell electrical performance. Due to its unique compatibility with FD devices, FB memory technology is fully portable to all forms of 3D device architectures such as fin-shaped field-effect transistors (FinFETs); multiple-gate FETs (MuGFETs); surrounding gate transistors (SGTs); and tri-gate, vertical double-gate and gate-all-around structures. For example, Figure 7 shows the programming window and retention time of an experimental 11nm FinFET device.

See DRAM Scaling page 44
Singapore’s Semiconductor Industry: A Vibrant Ecosystem

Ng Siew Kiang, Executive Director, Contact Singapore

A world-class technological hub located at the crossroads of Asia, Singapore is a vibrant electronics and research and development (R&D) growth engine, and is home to various multinational corporations.

The electronics sector is the backbone of Singapore’s manufacturing industry, generating S$67.9 billion (US$48 billion) in output and employing about one-fifth (92,000 workers) of Singapore’s total manufacturing workforce.

**Vibrant Semiconductor Ecosystem with Full Value Chain of Activities**

Echoing the story of how Singapore transformed itself from a third-world country to a first-world country within the short span of 40 years, it is interesting to see how Singapore has successfully developed its semiconductor industry from hosting only one assembly and test plant in 1968 to the vibrant industry ecosystem it is today.

Today, Singapore is home to about 40 IC design companies, 14 silicon wafer fabrication plants and 20 assembly and test facilities which have employed 40,000 workers such as IC designers and R&D engineers. Today, Singapore is ranked second in the world (behind Hsinchu, Taiwan) in terms of fabrication capacity.

Other notable achievements include:

- 10.9 percent manufacturing output share of global semiconductor revenue.
- 16 percent share of worldwide fabless semiconductor output.

Many of the world’s renowned semiconductor companies have established their Asian operations in Singapore. They include the world’s top three foundries (TSMC through its joint venture with NXP, UMC and GLOBALFOUNDRIES Singapore; formerly Chartered Semiconductor Manufacturing)); nine of the world’s top 10 fabless IC design companies (Broadcom, Qualcomm, Xilinx, MediaTek, Marvell, Avago, LSI, ST-Ericsson and NVIDIA); four of the world’s top six subcontract assembly and test companies (ASE, STATS ChipPAC, UTAC and Amkor); and leading integrated device manufacturers (IDMs) (TI, STMicroelectronics, AMD, Infineon, NXP and Micron).
In addition, it is worth highlighting the significant progress Singapore’s semiconductor industry has made beyond manufacturing. Singapore’s location at the heart of Asia places it in close proximity with Asia’s growing semiconductor customer base and outsourcing partners. Top semiconductor companies from across the globe have selected Singapore as their base for supply chain management, manufacturing oversight and other regional headquarters’ activities. For instance, Marvell recently announced its newly expanded 100,000 square meters regional headquarters facility in Singapore that will undertake sales, technical support, design, IC assembly and testing amongst other functions.

**Manufacturing for the Future: Investments in R&D**

Singapore is establishing a reputation for itself as an R&D powerhouse. R&D spending by the electronics industry in Singapore increased from S$1.3 billion (US$0.92 billion) in 2006 to S$2.18 billion (US$1.54 billion) in 2007. Despite the global downturn, more than 700 new semiconductor R&D jobs have been created since 2008, including IC design positions.

Growth in R&D spending has been driven largely by private firms. For instance, Infineon invested S$400 million (US$282 million) to boost its R&D activities in Singapore. And STATS ChipPAC established an R&D centre to focus on through-silicon via (TSV) and embedded die technologies.

A new IC design research centre focused on “green” microchips and circuits that run on ultra-low power but perform faster will also be set up by June 2010. This centre seeks to build on Singapore’s excellence in IC design, and it will collaborate with world-renowned universities, top research institutions and companies such as Agilent Technologies. It aims to hire at least 20 top-notch scientists and researchers.

Singapore offers end-to-end R&D capabilities, including component-level IC design and semiconductor process R&D; system-level product design; firmware development; and industrial design. For example, Dell and HP use Singapore as a base for printing, imaging and computer peripherals design as well as networking and high-end server design, respectively. This creates valuable opportunities for semiconductor companies to work closely with their systems/original equipment manufacturing (OEM) customers on product development, and enable them to tap into a full range of electronics design capabilities and talent.

**New Growth Areas**

The semiconductor market is projected to continue on its growth path. In a November 2009 press release, global research firm Gartner forecasted 2010 semiconductor revenue to bounce back to the 2008 revenue level at $255 billion, a 13 percent increase from 2009.

Singapore is committed to developing a robust and sustainable critical mass of wafer fabrication plants and promoting IC design activities from leading IDMs and fabless companies, particularly in analog/mixed-signal and radio frequency IC (RFIC) design, where Singapore already has a strong track record.

In addition to analog/mixed-signal and RFIC, Singapore has identified four emerging areas with strong growth potential: green electronics, bioelectronics, plastic electronics and security. Singapore will leverage its existing base of core electronics capabilities and strengths in material physics and biotechnology to pre-position and develop the local semiconductor industry to ride on these waves of growth. Several semiconductor companies in Singapore are already working on these new growth areas. For example, STMicroelectronics has established a centre developing plastic electronics, which would have applications in electronic devices such as sensors, touch screens and flexible electronics displays.

And Philips Lumileds, one of the world’s top five light-emitting diode (LED) makers, has set up its first high-power LED wafer fabrication facility outside of Silicon Valley.

Singapore has also identified the need for urban, health and wellness solutions, as Singapore and other cities worldwide continue to face the constraints and challenges of growing urbanization and rapidly ageing populations. The city plans to position itself as a “living lab” for companies to develop innovative and future-oriented solutions to these challenges, as well as create test-bedding platforms for testing and prototype development. Singapore’s ultimate goal is to serve as the reference site for the export of such solutions to global markets.

**Career Opportunities in Singapore’s Semiconductor Industry**

Semiconductor jobs are amongst the most highly paid in the manufacturing sector. Average remuneration for IC design, wafer fabrication and outsourced semiconductor assembly and test (OSAT) jobs is higher than the manufacturing sector by 68 percent, 37 percent and 11 percent, respectively.

The Singapore government is putting resources into developing the competencies of its future generation through a scholarship program for undergraduates and postgraduates. In 2009, the Singapore Economic Development Board established the S$16 million (US$11.3 million) IC Design Postgraduate Scholarship to train 150 IC designers with either a master’s or Ph.D. over five years as part of its efforts to train talent in the semiconductor industry.

In addition, there are opportunities for engineers and technicians to play a critical role in manufacturing, R&D, product and circuit design, and testing and assembly. According to the Strategic Skills List published in July 2008 by the Singapore Ministry of Manpower, the skills most in demand in the electronics industry are IC designer, media engineer and wafer fabrication engineer.

See Global Insights page 42
The ever-increasing design and process complexity of today’s embedded memories drives the need for robust test, repair and diagnostic solutions. Semiconductor companies are under incredible pressure to reach volume production with new designs in increasingly shrinking time windows, which intensifies the need for better support for yield learning and production ramp. And add to that all the low-power system-on-chip (SOC) designs requiring multi-dimensional optimization, increasing the complexity and embedded memory content per chip. The number of memory instances has also increased along with their hierarchical distribution. In addition, multiple embedded memory sources and embedded test and repair solutions—all on the same SOC—create major technological difficulties for designers.

In addition to design complexity, process complexity has also become a major challenge. The higher susceptibility to resistive, performance, bridging, parametric variation and other new fault types requires expanded test algorithms to detect, repair and diagnose these faults. A higher level of miniaturization requires better support for yield learning and production ramp-up. The ability to have on-the-fly monitoring and analysis of volume diagnosis data for increased efficiency of post-silicon bring-up, system debug and embedded memory characterization is now more critical than ever.

A powerful solution is needed to address these issues and provide designers with direct access and interactive communication with the internal circuitry of their SOC memory system, whether it is an internally developed or third-party memory, so they can debug and diagnose system issues more quickly during the chip bring-up process. Having the flexibility of mixing memories from various sources to meet specific design requirements, while using the most advanced test and repair solution, will help in the development of higher quality end products for their customers.

More faults are emerging at every new process technology—such as resistive faults, performance faults, bridging faults, parametric variation and so forth. To detect these faults, new algorithms are needed at advanced process nodes to diagnose, debug and classify the faults. Eliminating fault escapes will result in optimal product quality.

Other unique capabilities that designers need include the ability to extract embedded memory contents, to perform multi-corner characterization, and to assess reliability and temperature dependencies. Users should be able to classify and correlate defects, analyze redundancy utilization and precisely localize physical failures by zooming into the physical structure and locations of memory instances based on retrieved memory failures, as opposed to simply reporting the logical address of failed cells. With this type of solution, design and test engineers could dramatically simplify the chip bring-up process, in addition to accelerating the process.

Extending the value to the test floor for design and manufacturing test automation, a solution that offers the capability to support advanced process nodes such as 40nm would be desirable. And a highly intuitive user interface to enable users to quickly create complex test patterns and analyze silicon response results would be key. It would also need to rapidly generate detailed reports, hierarchically analyze, and quickly identify failure types and locations as designs are readied for transition from first silicon to volume manufacturing—analyzing large volumes of data and collecting and classifying statistical failure data at the die, wafer and lot levels.

To do this, designers are going to need a solution that offers advanced features:

- An optimal distribution of design-for-test (DFT) logic between the soft embedded memory test and repair system and the memory hard macro.
- Low clock frequency transitions to deliver greater power savings.
- A library of test operations and algorithms that target fault mechanisms and defect types associated with shrinking technology and leakage defects.
mSilica supplies system-centric mixed-signal power management ICs to the light-emitting diode (LED) backlight market. This broad-based and rapidly growing market includes liquid crystal display (LCD) TVs; specialty panels (industrial, military, instrumental and avionics); and general illumination (commercial, residential, industrial and government). mSilica’s LED display drivers utilize a proprietary and patent-protected combination of analog and digital circuit techniques. The company’s products embody a system-centric approach and provide on-chip solutions for local and global dimming, power management, signal conditioning and smart interfacing. This allows electronic equipment manufacturers to significantly enhance product features, while improving power efficiency, reliability and cost/performance.

Founded in 2006, the company has raised over $20 million in two rounds of funding. mSilica is engaged with leading users of LED backlighting ICs worldwide and is shipping its products in production volume. mSilica’s team comes from leading analog and mixed-signal semiconductor companies. Their combined experience empowers the company to deliver industry-leading products based on detailed system-level expertise, proven IC design know-how and extensive customer application knowledge. Headquartered in Santa Clara, California in the heart of Silicon Valley, mSilica offers worldwide technical support through its headquarters and offices in Korea, Japan and Taiwan. The company also supports its customers with sales representatives and distributors throughout Asia, North America and Europe.

In February 2010, Octasic announced its second-generation Opus2 digital signal processor (DSP) core, a high-performance, ultra low-power, asynchronous DSP architecture optimized for baseband processing and multimedia transcoding. The Opus2 core, based on Octasic’s unique asynchronous Opus DSP architecture, offers the lowest power consumption available in a fully programmable, high-performance DSP. Incorporating the experience gained from extensive application development on Opus1 and improvements to the asynchronous design, Octasic has doubled the platform’s performance, while improving its power efficiency. For example, a single device based on Opus2 can provide all the necessary processing for a complete 64-user High-Speed Packet Access+/Long-Term Evolution (HSPA+/LTE) base station while consuming less than 2.5W.

At Mobile World Congress, Octasic demonstrated an integrated reference platform with partners Continuous Computing and Analog Devices to wireless developers looking for high-performance, low-power solutions for their picocell and femtocell 3G applications. Opus2 is fully supported by a rich, highly integrated software development environment that includes an optimizing C compiler and timing-accurate simulator. Opus2-based devices will be available from Octasic later this year for use in wireless baseband, media gateway, private branch exchange (PBX) and video products.

“Octasic joined GSA in 2006 to connect with other members and gain valuable information and insight into the industry. GSA provides us with various forums to network with players in the semiconductor industry and helps us identify new market opportunities and drive our growth.”

– Robert Blake, Chief Executive Officer, Octasic
On December 10, 2009, GSA hosted its 15th annual Awards Dinner Celebration at the Santa Clara Convention Center in Santa Clara, California. At the event, companies were recognized for demonstrating outstanding performance in 2009. The theme for this year’s celebration was “Innovation: A Blueprint for Global Change.” The evening began with a networking reception that led into dinner before Jodi Shelton, president of GSA, took the stage.

The ceremony started with a greeting from Ms. Shelton and her introduction to a video showcasing the event’s title sponsor, TSMC. After the video presentation, Shelton introduced the evening’s keynote speaker, author of “Freakonomics” and “SuperFreakonomics” Steven Levitt. If the laughter and applause in the audience was any indicator, it was a very enjoyable speech.

Ms. Shelton then returned to the stage with GSA’s board chairman, Dwight Decker. They each shared their thoughts on the state of the industry after a tumultuous year. Shelton stated, “Even during the darkest period of this recession, the innovative spirit that is the foundation of semiconductor advancement was alive and well. The innovators, mavericks and visionaries in this industry did what they do best—innovate.”

Shelton and Decker then announced that he was handing off board chairmanship to Dr. Nicky Lu, chairman and chief executive officer of Etron Technology. They also announced the election of new board vice chairman, Joep Van Beurden, chief executive officer of CSR. Following both announcements, Dr. Lu and Ms. Shelton presented a gift to Mr. Decker for his seven years of service on the GSA board of directors. Mr. Decker said he was leaving “feeling confident in the future of GSA.”

After Mr. Decker left the stage, Dr. Lu commented that he has “some big shoes to fill” and that he is “committed to promoting an expanded scope and vision for GSA and to continue our vital work as a global neutral platform of cooperation.” After a few more comments from both Ms. Shelton and Dr. Lu regarding GSA’s goals for 2010, they encouraged the audience to relax and enjoy the awards ceremony.

Start-Up to Watch Award

To begin the ceremony, Scott McGregor, president and chief executive officer of Broadcom, and Aiman Kabakibo, chief executive officer of SiPort, announced the Start-Up to Watch Award winners Ambarella (accepted by President and Chief Executive Officer Fermi Wang) and Silicon Mitus (accepted by Chief Executive Officer Dr. Youm Huh). GSA’s Start-Up to Watch Award Committee selects the award winners by identifying the semiconductor companies that demonstrate the potential to positively change its market or the semiconductor industry through the innovative use of semiconductor technology or a new application for semiconductor technology.

Outstanding Financial Performance by a Private Semiconductor Company Award

The top five private semiconductor companies (in terms of growth percentage) that doubled revenue over eight consecutive quarters were eligible to receive an award for their outstanding financial performance. Due to confidentiality, private companies submitted their ballots directly to a designated consulting firm to determine which companies doubled revenue.

Bob Bruggeworth, president and chief executive officer of RF Micro Devices, and Sailesh Chittipeddi, co-president of Conexant, presented the Outstanding Financial Performance Award to ApexOne Microelectronics (accepted by Chief Executive Officer and President James Gao), Telegent Systems (accepted by Chief Executive Officer and Co-Founder Sam Sheng), and Xelerated AB (accepted by Chief Executive Officer Thomas Axelsson).

Most Respected Private Semiconductor Company Award

Greg Lang, president and chief executive officer of PMC-Sierra, and Ron Jankov, president and chief executive officer of NetLogic Microsystems, presented the Most Respected Private Semiconductor Company Award to Dr. Naveed Sherwani, chief executive officer of Open-Silicon. This award is designed to identify the private company garnering the most respect of the industry in terms of its products, vision and future opportunity. GSA’s Awards Committee reviewed all private semiconductor companies to select nominees, and online voting took place to allow members of the semiconductor industry, including chip companies and partners, to cast a ballot for the private semiconductor company they most respect.
Dr. Naveed Sherwani, chief executive officer at Open-Silicon, accepted GSA’s Most Respected Private Semiconductor Company Award.

Regional Awards: APAC Leadership Council Award and EMEA Leadership Council Award

This year GSA added two new awards to the ceremony. Dr. Huh, chief executive officer of Silicon Mitus, returned to the stage with Dr. Kishore Seendripu, chief executive officer and co-founder of MaxLinear, to explain that these awards focus on exceptional companies headquartered in the Asia-Pacific, Europe, Middle East and Africa that demonstrate the most strength in market leadership/competition, product lines, innovation, corporate management and overall likelihood of long-term success.

Dr. Huh presented the APAC Leadership Council Award to MediaTek (accepted by Vice President Lawrence Loh). David Baillie, chief executive officer of CamSemi, then presented Dialog Semiconductor with the EMEA Leadership Council Award (accepted by Chief Executive Officer Dr. Jalal Bagherli).

Analyst Favorite Semiconductor Company Award: Deutsche Bank Securities and Needham & Company

Ross Seymore of Deutsche Bank Securities presented the Analyst Favorite Semiconductor Company Award to Doug Bettinger, chief financial officer at Avago Technologies. Mr. Seymore stated, “Completing a successful IPO in such a difficult year is a truly unique accomplishment.”

Quinn Bolton of Needham & Company presented the Analyst Favorite Semiconductor Company Award to “the fastest growing company in our coverage universe,” Cavium Networks (accepted by President and Chief Executive Officer Syed Ali). He explained that “given Needham’s focus on emerging growth companies, the criteria used to select this year’s nominees is compound annual growth rate from 2008 to 2011.”

Most Respected Public Semiconductor Company Awards

Most Respected Emerging Public Semiconductor Company Award

The Most Respected Emerging Public Semiconductor Company Award is designed to identify the company garnering the most respect of the industry in terms of its products, vision and future opportunities. The criteria for this award include (but is not limited to) achieving up to $499 million in annual sales. In addition, profitability and market capitalization, among other financial and product successes, are considered to be listed on the ballot. Again, GSA’s Awards Committee reviews the companies meeting the criteria, and online voting took place to allow members of the semiconductor industry to cast a ballot for the public emerging semiconductor company they most respect.

Group President of Maxim Integrated Products Vijay Ullal and Vice President of Global Supplier Management, CVCM, Cisco Systems Ltd. Prentis Wilson presented the Most Respected Emerging Public Semiconductor Company Award to NetLogic Microsystems (accepted by President and Chief Executive Officer Ron Jankov).

Most Respected Public Semiconductor Company Award: Achieving $500 Million to $10 Billion in Annual Sales

John Park, president and chief executive officer of Dongbu HiTek, and Marianne Baldrica, managing director at NASDAQ OMX, presented this award to Broadcom (accepted by President and Chief Executive Officer Scott McGregor).

Most Respected Public Semiconductor Company Award: Achieving $10 Billion or More in Annual Sales

Richard Williams, president, chief executive officer and chief technology officer at Advanced Analogic Technology, and Doug Grose, chief executive officer of GLOBALFOUNDRIES, presented this award to Intel (accepted by Vice President and General Manager of Manufacturing and Supply Chain Brian Krzanich).

Best Financially Managed Semiconductor Company Award

The final company award of the evening was presented by Oleg Khaykin, chief executive officer of International Rectifier, and Dr. Craig Barratt, president and chief executive officer of Atheros Communications. The Best Financially Managed Semiconductor Company Award is designed to evaluate the financial health of public semiconductor companies based on a number of financial metrics, such as return on investment, return on equity, inventory turns, revenue, net income, days sales outstanding, cash per share, cash burn, gross profit margin, operating margin and current ratio. GSA and financial analysts evaluate each company against their peers, and the one with the best overall performance is determined the winner.

The Best Financially Managed Semiconductor Company Award winner was Linear Technology (accepted by Chief Executive Officer Lothar Maier).
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ocial media sites, such as YouTube, Twitter and Facebook, present significant opportunity for individuals and businesses to communicate to extensive numbers of people in ways never before envisioned. Facebook, for example, currently boasts more than 350 million users, and conservative estimates show at least 18 million Twitter users. These numbers are only expected to increase over time. While these sites present tremendous growth opportunities for businesses, they have sparked a flurry of activity among IP owners who are scrambling to find ways to safeguard their valuable assets. While the title of this article may appropriately describe the reaction of an IP owner upon discovery that it has been victimized on a social media site, there is no need to panic. There are various tools available to the IP owner that can be used to address abusive situations. Naturally, the first question an IP owner must ask is “How much of this can I take?” When the answer to that question is “no more,” the owner is invited to turn to this article—which is intended to begin identifying answers to some difficult and challenging questions.

Part 4 of 4: You Twit Face! Protecting your IP in the World of YouTube, Twitter and Facebook: A Practical Protection Guide for the IP Owner

In 2009/2010, GSA brought GSA Forum readers a four-part series analyzing legal issues such as antitrust, bankruptcy, immigration and, now, intellectual property (IP) protection. These articles were written by Gardere Wynne Sewell LLP, one of the Southwest’s largest full-service law firms providing legal services to private and public companies and individuals in areas of energy, litigation, corporate, tax, environmental, labor and employment, IP, governmental affairs and financial services.

While GSA does not endorse any particular perspective, we believe whether you agree or disagree, these articles will encourage semiconductor companies and their partners to ask and begin identifying answers to some difficult and challenging questions.

A few points to keep in mind. The IP owner always has at its disposal the option of pursuing formal legal remedies, such as initiating a lawsuit, to protect its valuable IP assets. But given the significant expense, resource and time commitments associated with litigation, the IP owner would be well-advised to consider, at least as a first option, utilizing the dispute resolution procedures set up by the specific social media site. Remember that each social media site (such as Facebook and Twitter) is run by a company—not the government, not a court. Because these are different companies, their procedures and policies for addressing abusive situations, while similar, are not the same. The different policies and procedures do, however, echo a common theme of “self-interest” in that each company does not

want to be sued by IP owners over infringing content. Clearly, it is in the companies’ best interest to work with IP owners to address acts of infringement occurring on their sites. If a site fails to act after being put on notice of the infringing activity, the social networking site runs the risk of being charged with being complicit in the infringement. This provides a significant advantage to IP owners and certainly increases the chances of getting the issue resolved quickly.

YouTube

Anytime there is an open forum inviting expression, such as with YouTube’s “self-broadcasting” site, this increases the potential for abusive situations. Of course, despite YouTube’s encouragement to patrons to “Broadcast Yourself™,” YouTube recognizes that certain “expression” is not permitted, especially when that expression trades on others’ rights. In fact, YouTube expressly states in its Terms of Service that it “does not permit copyright infringing activities and infringement of IP rights on its Web site,” and if such activities take place, YouTube will remove any infringing content from the site. Granted, most social media sites state in their Terms of Service that the company reserves the right to make the call whether content is infringing or not, and reserves the right to remove (or not remove) the complained-of content. With that said, more often than not, if the content looks to be infringing (even if it is a close call), the company is going to remove the content due to the threat of being sued if wrong. As such, if an IP owner finds someone else trading on its rights on a social media site, the owner should take immediate action. The IP owner has spent years and resources developing these rights, and while it may be inconvenient for the IP owner to go through the process to correct the wrong, it must be done.

The first step that the IP owner will want to take is to set up an account with the social networking site. In most cases, this is a free service and usually necessary to utilize the provider’s dispute mechanisms. The next step will be to determine under which “category” the abusive conduct fits. As an example, if someone posts

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on YouTube a video that is a copy of the IP owner’s video, that is a copyright violation, and the rules set out for addressing copyright violations must then be followed. On the other hand, if someone uses the IP owner's brand name or company identifier as a user name, or in such a way as to cause confusion among consumers, that is a trademark issue, and the trademark rules set out on the particular site must be followed. Due to the relatively recent passage of the Digital Millennium Copyright Act (DMCA)—which gives online providers specific protections if certain rules are followed such as designating a specific “copyright agent” to receive complaints—more sophisticated social media sites will likely have a specific section in their Terms of Service for addressing copyright disputes. This does not mean that the company will not entertain requests to address other forms of IP disputes, such as trademark and rights of privacy issues. It just means that the procedure for addressing non-copyright disputes often will be buried within the Terms of Service and may be difficult to find.

As an example, YouTube provides under the heading “Copyright Infringement Notification,” (http://www.youtube.com/copyright_complaint_form) a questionnaire asking “What is the issue?” Depending on what box is checked (e.g., privacy, trademark infringement, copyright infringement, inappropriate content [nudity, violence], abuse/harassment, rights of publicity issues), the IP owner is directed to the specific section of YouTube’s Web site which addresses the specific type of infringement.

Twitter

On Twitter, “You are what you Tweet.” That means “What you say and do on Twitter can and will be used against you.” There is a growing trend for not only individuals but also businesses to use social media sites, such as Twitter and Facebook, as means for connecting with business prospects. Like YouTube, Twitter devotes a specific section of its site to copyright violations (http://twitter.com/tos, under “Copyright Policy”), including designating a specific “Copyright Agent” to receive DMCA requests in accordance with a specific DMCA procedure. One of the most common violations occurring on Twitter’s site relates to trademark and business name squatting. According to Twitter’s Trademark Policy, any use of a company’s business name, logo or other trademark-protected material in a way that may mislead or confuse (even if it does not rise to the level of technical “trademark infringement”) constitutes a trademark violation. In most cases, Twitter will work with an account owner to remove the infringement and will allow the account holder to keep his or her account. But Twitter reserves the right to permanently suspend an account if Twitter determines (in its discretion) that there is a “clear intent to mislead people.”

If the IP owner has a Twitter account, it can use Twitter’s “support ticket” system to report trademark violations (http://twitter.zendesk.com/forums/26257/entries/18367). As an alternative, abusive situations can be reported by sending an e-mail to terms@twitter.com along with the following information:

- Username of the violating account (or the URL to their profile page).
- Company name/company Twitter account (if applicable).
- First and last name.
- Title.
- Address.
- Phone.
- Fax.
- Company domain address.
- Contact’s company domain e-mail address.
- Trademark registration number (if applicable).
- The requested action (e.g., removal of infringing account or transfer of trademarked username to an existing company account).

Facebook

When an individual or business signs up for a page on Facebook, the user agrees to Facebook’s Statement of Rights and Responsibilities in which the user agrees, among other things, not to “post content or take any action in Facebook that infringes or violates someone else’s rights or otherwise violates the law.” In this agreement, it is acknowledged that Facebook “can remove any content or information” if Facebook believes it violates the provisions of the Statement. Like the YouTube and Twitter policies previously described, Facebook provides separate mechanisms for reporting copyright and non-copyright infringement issues. For copyright infringements, the IP owner is directed to fill out and submit an automated DMCA form (http://www.facebook.com/terms.php?ref=pf#legal/copyright.php?copyright_notice=1).

In connection with Facebook’s recent policy change toward user names, Facebook has developed a specific form used to report infringing user names (http://www.facebook.com/help/?search=username#help/contact.php?show_form=username_infringement).

Naturally, it is in the best interest of the provider to act quickly, but as is the case with many providers, oftentimes, “quickly” can take some time. Facebook provides on its Web site that “So long as everything appears to be in order, we will promptly remove or disable access to the [infringing] content.” To this end, IP owners are encouraged to be diligent in following up with the providers to make sure their requests are being addressed.

Conclusion

While the advent of social networking sites has created an additional arena that IP owners must police for infringing activity, there are cost-effective tools provided by social media provider Web sites to assist IP owners in protecting their rights. IP owners would be well-advised to implement internal procedures for monitoring the content of social networking sites, for example, by periodically searching these sites for “keywords” attributable to the IP owner or its company. If the IP owner finds itself in a situation involving abusive conduct by others, the IP owner should take immediate action. As previously described, this involves informing the provider of what IP rights are infringed and how the content infringes those rights. The dispute mechanisms provided by these providers are excellent, cost-effective ways of protecting an owner’s valuable IP rights. If the issues cannot be resolved by using these mechanisms, the IP owner may be forced to pursue other legal remedies, but such measures should only be resorted to after fully utilizing the specific dispute procedures set out by the providers.

About the Authors

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An inside look at innovative semiconductor start-ups

The Q4 2009 revenue numbers are rolling in, and it’s clear that the semiconductor industry has made a miraculous recovery from an unprecedented low in 2008. Some would say it’s a jobless recovery and that the strong generally got stronger while several weaker players withered away. Such is the law of the jungle.

If top-line revenue growth, cost cutting and free cash flow were the focus for 2009, what does that mean for innovation? Even with semiconductor investment at historic lows, more than a few areas saw major progress. Light-emitting diode (LED) innovation is pressing on as the world embraces solid-state lighting. Many companies are driving the migration from III-V processes to lower cost, higher integration CMOS for wireless power amplifiers (PAs) and front-ends. In general, wireless continues to see much activity, ranging from front-end to baseband, low-frequency radio frequency identification (RFID) to 60GHz, and miles to millimeters. The next generation of high-speed links is beginning to emerge, including Universal Serial Bus (USB) 3.0, 60GHz wireless and Intel’s LightPeak 10G high-speed optical cable technology.

Video continues to see innovation in areas such as mobile video communications, codec standards, and 3D and Quad-HD displays. Although not a semiconductor, but intimately related, the pace of battery innovation is increasing, from automotive- to chip-scale batteries. 2009 was the year of the consumer microelectromechnical systems (MEMS) gyroscope, and the pace of MEMS innovation is accelerating. Lastly, the printed electronic industry is still in its infancy, but making great strides.

With all that said, my favorite start-up during last quarter was Energy Micro AS, a company founded in 2007 to develop “the world’s most energy friendly microcontrollers.” Those that know me know I am not a fan of new processor architectures. They are a dime a dozen, success is rare and graveyards are littered with commercial failures. The microcontroller arena is also subject to the market power of incumbents, channel breadth and depth, and challenges related to building scale based on thousands of low-volume designs.

Countering these points, Energy Micro uses the industry-standard ARM Cortex-M3 architecture, leveraging ARM’s dominance and tool chain. And the company is already engaged with high-volume customer partners.

Energy Micro is 100 percent owned by its founders and employees, and has raised a scant US$6 million to date. I like capital efficiency, sweat equity and when founders’ capital is on the line. The founders hail Chipcon, which they sold to TI for $200 million in January 2006. Prior success is worth a lot.

In talks with the company, it is clear that they have really thought through the issue of power consumption, not only addressing one or two issues, but approaching it as a comprehensive, holistic and system- and application-level problem. Energy Micro’s EFM32 Gecko microcontroller family incorporates numerous energy-saving features such as peripheral operation without central processing unit (CPU) intervention and, while the CPU is sleeping, fast wake-up, ultra-low standby current, multiple energy modes, ultra-efficient peripherals and low active mode current consumption.

Energy Micro argues that its innovations in the EFM32G have been proven to extend battery life by a factor of four, compared to existing 8-, 16- and 32-bit microcontrollers from companies such as TI, Silicon Labs, NXP, ST, Microchip and Atmel, whether based on proprietary or standard architectures such as the 8051 and ARM Cortex-M3 and M0.

The EFM32G family is comprised of 22 different microcontrollers with a variety of features such as an analog-to-digital converter (ADC), DAC, liquid crystal display (LCD) controller, timers, general purpose input/output (GPIO), universal asynchronous receiver/transmitter (UART), direct memory access (DMA) and advanced encryption standard (AES) block. The devices are available in a variety of packages and are fabricated by TSMC in an 180nm process.

The devices have been designed in close partnership with leading companies within the energy metering, home and building automation, alarm and security, and medical systems industries. Energy Micro believes that these applications collectively comprise a billion unit opportunity.

The first products are currently sampling with lead customers. Kamstrup A/S, a leading European energy metering company, plans to introduce products containing the EFM32 in 2010. VELEX A/S, one of the strongest brands in the global building materials and home improvement industry, is also an early partner customer.

A large, growing market opportunity, comprehensive product family, product shipment and customer wins in a few short years with only $6 million in capital is quite impressive. That’s why Energy Micro is my pick this quarter.

Geir Forre, President and CEO
Øyvind Janbu, CTO
Eirik Jørgensen, VP, Engineering
John Helge Fjellheim, VP, Worldwide Sales
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Cliff Hirsch (cliff@pinestream.com) is the publisher of Semiconductor Times, an industry newsletter focusing on semiconductor start-ups and their latest technology. For information on this publication, visit www.pinestream.com.
**Dr. Morris Chang Exemplary Leadership Award**

The final award presentation of the evening was the Dr. Morris Chang Exemplary Leadership Award. This award recognizes individuals, such as its namesake, Dr. Morris Chang, for their exceptional contributions to drive the development, innovation, growth and long-term opportunities for the semiconductor industry.

The recipient of the 2009 Dr. Morris Chang Exemplary Leadership Award was Dr. Aart de Geus, chairman and chief executive officer of Synopsys. Since co-founding Synopsys in 1986, Dr. Aart de Geus has expanded Synopsys from a start-up synthesis enterprise to a world leader in electronic design automation (EDA). He has been honored for his industry achievements with several awards, including the 2001 IEEE Circuits and Systems Society Industrial Pioneer Award, 2007 IEEE Robert N. Noyce Medal and the 2008 EDAC/CEDA Kaufman award. Dr. Aart de Geus is active in the business community as chairman of the board of the Silicon Valley Leadership Group (SVLG), and is a member of TechNet, the Global Semiconductor Alliance (GSA) and the Electronic Design Automation Consortium (EDAC). He is also heavily involved in education for the next generation, creating the Synopsys Outreach Foundation in 1999, which promotes project-based science and math learning throughout Silicon Valley.¹

GSA was excited to have Dr. Morris Chang himself in attendance to present the award to Dr. Aart de Geus. As he presented the award, Dr. Chang said, “Aart has extraordinary business vision which laid the foundation for building one of the industry’s most important partners, Synopsys. He is an intellectual innovator that we depend upon to propel this industry forward… GSA is proud to present its most prestigious award to Aart.”

Traditionally, the evening would then come to a close with a champagne toast and well wishes for 2010. However, this year, Dwight Decker and the GSA board of directors had a surprise for Ms. Shelton. As Dr. Nicky Lu presented Ms. Shelton with a gift, Mr. Decker said, “We are taking this opportunity to recognize you for the visionary you truly are and 15 years of hard work and dedication to this industry.”

Ms. Shelton then gave her thanks and invited key industry leaders to join herself and Dr. Lu and Mr. Decker on stage for the champagne toast to welcome the New Year.

The support of our title sponsor, TSMC, as well as our general sponsors, ARM, Advantest, Amkor, ASE Group, Atheros, Broadcom, Cadence, Chartered, Deutsche Bank, Dongbu HiTek, eSilicon, GLOBALFOUNDRIES, IBM, Inphi, J.P. Morgan, MagnaChip, Morgan Stanley, Needham, nVIDIA, PricewaterhouseCoopers, ON Semiconductor, Qualcomm, Samsung, SAP, Synopsys and UMC, is what made this event a great success!

Be sure to join the celebration next year! Mark your calendar for the 2010 GSA Awards Dinner Celebration on December 9, 2010 at the Santa Clara Convention Center, Santa Clara, California.

**Resources**

¹[http://www.synopsys.com/COMPANY/ABOUTSYNOPSYS/Pages/ExecutiveManagement.aspx](http://www.synopsys.com/COMPANY/ABOUTSYNOPSYS/Pages/ExecutiveManagement.aspx)

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### Optimization continued from page 32

- A special user logic handshake interface that allows for easy handling of multiple power domains and voltage islands on-chip.

**Figure 3. A Complete RTL to Test Floor Embedded Memory Test and Repair Solution**

With advanced automation capabilities to interactively communicate with the embedded test and repair system infrastructure in a chip through a JTAG port for post-silicon bring-up, system debug, diagnosis and characterization of embedded memories, the extraction of memory contents, multi-corner and multi-voltage characterization, precise physical failure localization, defect classification and redundancy utilization analysis would be possible—all from an engineer’s desktop without utilizing expensive automatic test equipment.

**Summary**

What designers really need is an end-to-end yield optimization solution that includes intellectual property (IP), design automation and manufacturing automation to address the design and process complexity challenges they face today—from initial design planning all the way through post-silicon bring-up and volume manufacturing.

**About the Author**

Dr. Yervant Zorian has served as Virage Logic’s vice president and chief scientist since joining the company in 2000. Prior to Virage Logic, Dr. Zorian served as a distinguished member of the technical staff at Lucent Technologies and Bell Laboratories and chief technical advisor to LogicVision. Dr. Zorian also serves as vice president of the IEEE Computer Society for Conferences and Tutorials and is the editor-in-chief emeritus of IEEE Design & Test of Computers. He founded and presently chairs the IEEE 1500 standardization working group for embedded cores, and has authored over 250 papers and four books. Dr. Zorian has received a number of best paper awards, is an honorary doctor of the National Academy of Sciences of Armenia, is a fellow of the IEEE and is the recipient of the 2005 IEEE Industrial Pioneer Award. Dr. Zorian received his master’s from the University of Southern California and a Ph.D. from McGill University. You can reach Dr. Yervant Zorian at yervant.zorian@vingelogic.com or 510-360-8035.
PCM technology to the market. The first effort involves reaching out to our current NOR and NAND customers to identify what PCM’s increased functionality can provide them in terms of enhancing applications or reducing bill of materials (BOM). The second effort, as I previously mentioned, is to penetrate the computing market. The memory hierarchy in computing is already being changed by applications such as SSDs, so I believe the time is ripe to analyze alternative ways of architecting memory subsystems in computing platforms. We have received positive feedback from numerous data processing original equipment manufacturers (OEMs) that believe PCM has a strong value proposition in the industry.

Q: The commercial use of NVM technologies (e.g., ferroelectric RAM (FeRAM), PCM and magnetoresistive RAM (MRAM)) has been slow as their long-term reliability and scalability needs to be established. However, these technologies are starting to break ground as developers have made significant improvements in the technologies’ level of integration and performance. What customer barriers must be overcome for these alternative technologies to potentially gain market share? What are the main challenges these new technologies face when competing with established memory technologies?

A: Aside from the fundamental technical challenges of new technologies, the barriers to adoption are generally related to cost and where in the system the memory sits. These two factors certainly influence the ability of customers to ramp new technologies.

Regarding cost, to gain market interest, I believe the alternative technology’s expense must be five to 10 times lower than its competitors’ if there is no other value proposition offered. As an example, PCM’s cost is certainly not five to 10 times lower than its competitors’, so Numonyx focuses on conveying the value of PCM’s features to consumers. Compared to DRAM, PCM is much more energy-efficient. When no information is being read or written, there is no power consumption. Further, PCM’s write endurance is far greater than NAND’s and NOR’s. As NAND and NOR scale, their limitations primarily arise from the fact that the number of times you can write to these technologies generation after generation is starting to shrink. We believe these benefits that set PCM apart from other memory technologies will allow it to gain significant market share in today’s industry despite its costly price tag.

The time it takes for a new memory technology to be employed depends on if it is on a memory bus or abstracted interface. If a memory technology is on a memory bus (e.g., DRAM bus and NOR bus) that requires software and hardware changes, it generally takes a far greater amount of time to make these modifications. Additionally, multiple costs involving expense, risk and time arise. On the other hand, if a memory technology is on an abstracted interface (e.g., SSD and memory card), it is much easier for a customer to potentially adopt a new technology as they have the ability to test it and make sure it meets their performance and reliability requirements. However, the downside to this is that most abstracted memory devices/technologies are data technologies which are usually measured on a dollar per gigabyte basis.

The main challenge new technologies face when competing with established memory technologies deals with a cost/value trade-off. As I previously mentioned, if a new technology is more costly than a traditional technology, then it better possess great value that customers are willing to pay for. An alternative, disruptive technology such as FeRAM has never heavily saturated the market because the technology wrestles with a severe cost disadvantage compared to NOR and offers no real value proposition. With PCM, Numonyx has been working with customers over the past several months to get them over the hurdles required to accept a new technology based off of what we think is a reasonable balance of cost and benefit.

Q: Today’s industry is seeing many hard disk drive (HDD) manufacturers enter the crowded, competitive SSD market. Gartner estimates unit growth of enterprise SSDs to double and its sales to reach $1.0 billion in 2010. With NAND forecasted to generate more than 20 percent of Numonyx’s revenue in 2009, what potential do you believe the SSD market holds in driving NAND demand? Do you believe SSDs will eventually replace HDDs in the PC market?

A: The SSD market is currently in its infancy phase, so its growth potential is great and could go through the roof. I believe the adoption rate of SSDs will dramatically increase in 2H 2010, making it an interesting time for the NAND industry. We are certainly keeping a close eye on the SSD market because if the demand for SSDs exceeds capacity, then the impact on average selling prices (ASPs) will be dramatic.

It has taken the industry longer than expected to fully comprehend the true value of SSDs over HDDs. Over the next couple years, I believe SSDs will gain significant share of the PC market. The cost/value trade-off I discussed earlier comes into play with SSDs. It is well known that SSDs cost more per gigabyte than HDDs. I recently paid 7 cents a gigabyte for 1.5 terabytes, totaling only $105 for a HDD. SSDs are clearly not as cheap, but there is value in its cost of ownership (i.e., cost to build and maintain it and liabilities) and performance. There is something extremely nice about picking up my laptop without shutting the lid and walking around the office, conference room to conference room, without worrying about crashing a hard drive. Over the next couple quarters, I predict SSD builders will create a new price point with a lower density SSD that will have more than enough density for consumers in the workplace.

Q: As 3D technology furthers the advancement of transistors, through-silicon via (TSV) wafers are predicted to represent 25 percent of the
memory business by 2015, creating great technological changes within the memory market. What do you see 3D technology developing in the next five years? What challenges arise with 3D TSV technology?

A: When I worked at Intel in the late 1990s, the push we got from customers (primarily wireless customers) to integrate more silicon per square millimeter was incredible, and as a result we pioneered many chip scale and multi chip packages. There will be further requirements to improve upon existing, simple processes such as stacking chips. I cannot forecast what percentage TSV wafers will represent in Numonyx's business or the industry's business in 2015. But I do know that the requirement to adapt and make changes will always be there, and as a memory supplier, we will be ready for it.

One of the main challenges of 3D TSV technology is, of course, cost. In the memory business, we must be able to provide this technology at a low cost. As well, clearly, there are the original technical challenges we faced when we first started stacking chips, and we need to make sure there aren't any new challenges. As engineers, it will be our job to solve that.

Q: The semiconductor initial public offering (IPO) market is showing positive signs of recovery as four semiconductor companies filed in November 2009. As a company that expects to be profitable in the coming quarters and with a healthier IPO environment, has Numonyx pondered growing its business by going public? Looking forward, what other expansion strategies has the company considered implementing?

A: After working at two public companies, I believe there are many benefits available to a private company. As a new company, we are currently enjoying those benefits. Of course, there is always the possibility of becoming a public company in the future, but we have no plans to file an IPO at this time.

I believe that PCM's numerous benefits (i.e., high read/write speeds, low volatility and high storage density) will allow the company to develop and enter new, untapped markets. I strongly believe that using PCM technology to penetrate these markets will help drive Numonyx's expansion and present us with many other future opportunities.
the proposed 3D IC technology, a new $1 billion fab can have the same production capacity compared with a conventional $4 billion wafer fab.

Combining four times higher production capacity from a 3D IC fab (or one quarter of fab investment for 3D IC processing) and about four times more die per wafer with 3D IC technology, memory productivity can increase up to 16 times. Therefore, with 3D IC technology for high-density memories and the new 3D IC fab business model, the memory business can overcome the high fab ownership cost, low ASP and low fab investment ROI.

Summary

The memory business model and its innovation through miniaturization face significant challenges. Therefore, a novel 3D IC architecture for high-density memories with high productivity, low processing cost, low die cost, unrestricted 3D interconnects with high bandwidth, and high-density memory cells should be considered for allowing Moore’s Law and the pace of memory scaling to be extended. A new memory business model using 3D IC processing will significantly reduce fab investment, maximize ROI and increase productivity sharply.

A typical annual package in Singapore includes a 13th month bonus and performance bonuses. Employers also contribute to an employee’s Central Provident Fund (CPF), which is a mandatory savings scheme that seeks to secure an employee’s financial future after retirement, and covers partial hospitalization, housing, family insurance and assets management.

A Great Place to Live

The 2009 HSBC Experience Survey results showed that expats voted Singapore the fourth-best country in the world to live and work. The expats were polled on their overall quality of life and ease of settling in. Many of them said they found standards in Singapore to be higher than those back home, and enjoyed the city-state’s superior food, transport and healthcare.

The HSBC survey results are reflective of the high quality of life that global talent can enjoy in Singapore. Singapore offers a well-developed infrastructure with a wide range of education, housing and healthcare choices suited to every budget. Coupled with the country’s low personal taxation rates, which are between 0 percent and 20 percent, Singapore is an affordable international career destination for those seeking to enter an exciting new phase in their lives.

About the Author

Siew Kiang is the executive director of Contact Singapore, a global alliance of the Singapore Economic Development Board and the Ministry of Manpower. Contact Singapore aims to attract global talent to work, invest and live in Singapore. For more information on working and living in Singapore, visit www.contactsingapore.sg. Job opportunities are also available at www.contactsingapore.sg/jobs.

Dieter K. Schroder is a professor in electrical engineering at Arizona State University. Prof. Schroder is an IEEE lifetime fellow and served as a distinguished national lecturer for the IEEE Electron Device Society from 1993 to 2007. He is the author of “Semiconductor Material and Device Characterization,” one of the best-selling texts in the semiconductor field. You can reach Dieter K. Schroder at schroder@asu.edu.
position of one central atom trapped in a tetrahedron of oxygen atoms. The central atom's position represents the stored bit state within the PZT ferroelectric molecule. Commercial FRAMs have been available for at least two decades, but like NAND Flash memories, FRAMs also exhibit wearout failure. More importantly, FRAM capacities remain small, and lithographic scaling may become a severe problem because ferroelectric materials tend to lose their ferroelectric properties when the amount of ferroelectric material used drops below a threshold value.

Phase-change memory (PCM) first appeared as a cover story in Electronics magazine nearly 40 years ago, but very few commercial PCM devices have been introduced so far. PCM stores bits as physical state changes in a chalcogenide glass that can take either a crystalline or amorphous form. In crystalline form, chalcogenide glass is a good electrical conductor. In the amorphous form, it's not. The conductivity difference produces a usable memory cell. Chalcogenide glass is the active material used for making recordable CDs and DVDs, so its crystalline/amorphous properties are very well understood by now. However, writing to a PCM cell literally involves melting and annealing glass, so PCM write cycles aren't particularly fast (approximately 100 microseconds at current lithographies); and PCM storage retention drops quickly as the operating temperature rises. Retention time for one vendor's prototype PCM cells is on the order of 10 years at 85°C but only 10 seconds at 165°C and 10 microseconds at 225°C. Similar to NAND Flash and FRAMs, cycling stresses cause wearout failure in PCMs, which have endurance ratings of approximately $10^8$ write cycles.

MRAM stores data in magnetic material introduced into the semiconductor cell. MRAM's big advantages are density, speed, symmetrical read and write cycle times, and infinite write endurance. The MRAM storage element, called a magnetic tunnel junction (MTJ), consists of a sandwich of one fixed (or “pinned”) magnetic layer and one switchable magnetic layer separated by an insulating layer to form a tunnel junction, as shown in Figure 2. Write currents switch the magnetic orientation of the switchable layer with a measurably different junction resistance depending on whether the magnetic polarities of the fixed and switchable layers are aligned or are opposed. The difference in resistance provides the readout of the cell's state. Memory chips manufactured in first-generation MRAM technologies are already available in the market.

Several memory vendors are also currently developing a new and different sort of MRAM technology dubbed spin torque transfer (STT). The STT memory cell employs special layers that uniformly polarize the spin of the electrons flowing through the MTJ, and the spin-polarized current imparts magnetic moment to the storage layer depending on the direction of electron flow through the cell. Significantly, an STT memory cell's write current shrinks with the square of the linear lithographic dimension of the MTJ, which suggests that shrinking lithographies will allow STT MRAMs to achieve NOR Flash memory densities and perhaps even approach single-level cell (SLC) NAND Flash memory densities. Note that MRAM has infinite write endurance, unlike competing non-volatile semiconductor memory technologies. Commercial STT MRAMs should be available within the next few years.

Table 1 compares significant attributes of various volatile and non-volatile memory technologies.

<table>
<thead>
<tr>
<th>Attribute</th>
<th>SRAM</th>
<th>DRAM</th>
<th>NAND-Flash</th>
<th>NOR-Flash</th>
<th>FRAM</th>
<th>PCM</th>
<th>MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-volatile</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Fast Read</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fast Write</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>High Endurance</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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</tbody>
</table>

If the RAID server’s primary memory cache—currently implemented with volatile DRAM—were inherently non-volatile, there would be no need for smaller non-volatile memories to hold the RAID server’s firmware, configuration data and the journal log file. NAND Flash could serve as the only memory a RAID server needed if it had faster read and write cycle times and if it were not susceptible to write endurance failures. Currently available and soon-to-be available MRAMs are already the best candidates for the RAID server’s journal and log files. STT MRAM, when it becomes available, will have all the required attributes needed to serve all non-volatile memory functions in the RAID server, including the primary RAID cache.

About the Authors
Barry Hoberman has held management positions at several technology companies, including founder and chief executive officer of inSilicon (now part of Synopsys) and chief executive officer of Virtual Silicon. His primary focus is in strategy and business development for semiconductors, semiconductor manufacturing and semiconductor intellectual property (IP). He has 13 U.S. patents and holds two B.S. degrees from the Massachusetts Institute of Technology. You can reach Barry Hoberman at bhoberman@crocus-technology.com.

Steve Cliadakis has over 20 years experience in business development, marketing and product development for technology companies, with a concentration in semiconductors and IP. He is the founder of Silicon Impact, providing business development and strategy services for start-ups and well-established companies. Cliadakis holds a B.E. in electrical engineering from the State University of New York at Stony Brook and an MBA from Adelphi University in New York. You can reach Steve at steve@siliconimpact.com.
but not with the same performance. We will continue to use 3bpc in consumer products, but not in systems. Single-level cell (SLC) and multi-level cell (MLC) will be used in SSDs. We are not comfortable using 4bpc technology. The 16-level 4bpc technology sacrifices too much reliability and performance and there is little cost benefit received. We believe it is only good for content.

**Q:** The demand for data security solutions has risen with the increasing amount of data stored in mobile devices. ABI Research predicts the mobile security market to surpass $4 billion by 2014. As a company that has recently begun to offer security storage solutions, do you feel that the integration of secure applications in mobile devices will soon be a requirement of consumer electronics suppliers?

**A:** Data security will definitely be a necessity in consumer electronics, and we have focused a great deal of our resources on this. We hope to provide a whole series of security products in the future as this is where the margins and market growth lies. However, it takes experience and reputation to address the security market as it is more closed than the open computer market. Phison currently offers security applications in cards and USB Flash drives. A series of SSDs with Advanced Encryption Standard (AES) crypto will join our offerings later.

The demand for authentication and security solutions will continue to drastically grow given the nature of cloud computing (i.e., all digital files stored in one area). We recently formed a joint venture with a veteran company in the security market which will leverage the strength from each company to successfully address the security market in cloud computing.

**Q:** According to C.J. Muse, an analyst at Barclays Capital, memory makers will finally increase capital expenditures in 2010 after a very difficult 2009, accounting for 42% of the chip industry’s capital spending. What might this spending increase trigger, and what markets will benefit?

**A:** Overspending might trigger another price slump, which proves good for some applications such as SSDs as they rely on a low price point to take off. Many people believe SSDs will take a significant share of the hard disk drive (HDD) market and will be able to address the optical market in the long run.

This is a very dynamic world; you never feel the current spending is enough when demand is there. All we can do is remain cautious and be very vigilant about market vibrations.

**Q:** The transition from using HDDs to SSDs in today’s industry promises increased performance and power value. However, the usage conditions and requirements of SSDs greatly differ from other devices that use NAND memory technology such as MP3 players and USB devices. Looking forward, what challenges do you feel SSDs will face with NAND technology?

**A:** I believe the performance of SSDs is much better than HDDs in terms of sequential data transmission, random input/output operations per second (IOPS), etc. However, the reliability of NAND Flash within SSDs is always a concern because SSDs are used in systems that store a large amount of important data. When the reliability of NAND Flash lowers as process scales, the SSD controller takes on the responsibility of maintaining system reliability. The SSD controller manages NAND Flash with advanced error-correction code (ECC), global wear leveling and multi-channel, which needs a large built-in cache. The challenge here is that when the cost of NAND Flash drops, the cost of the controller actually goes up. Not only is the built-in cache adding cost, but the R&D expense is also high, and it takes longer to develop the product.

Today, there are many SSD controller makers emerging, but I don’t believe these companies will survive because their profit will not outweigh the heavy R&D cost. Phison is in a much better position than others as we provide SSD-finished products in addition to controllers.

**Figure 7. Programming Window (Left) and Retention Time (Right) for a 11nm FinFET FB Memory**

For embedded applications, 3D structures are not necessary due to the larger footprint available for the bit cell. It is also possible to integrate capacitor-less RAM cells using planar transistors on FD SOI.

The main challenges with FB memory technologies are achieving the targeted retention times required by the application, integrating with a low-cost process for 3D implementations and operating at low voltage to satisfy all reliability requirements. The retention times demonstrated in Figures 4 and 6 satisfy the retention requirements for the typical bit cell. Future publications will disclose more information on 3D and low-voltage implementations.

**The FB Memory Bit Cell: The Future of High-Density Embedded and Standalone Memory Applications**

For technology nodes below 40nm, standard 1T/1C DRAM and 6T SRAM bit cells present huge scaling and manufacturing challenges. Due to the simplicity and performance of FB memory with future 3D structures, it appears to be the ideal candidate to replace standard RAM bit cells for future high-density embedded and standalone memory applications.

**About the Author**

In 2002, Dr. Pierre C. Fazan co-founded Innovative Silicon, developing a new SOI single-transistor memory technology. He acted first as chief executive officer and is now chairman and chief technology officer of Innovative Silicon. From 1989 to 1997, he worked as process integration engineer and then as manager at Micron Technology, Boise USA, focusing on DRAM process integration. In 1997, he was named Professor at the Swiss Federal Institute of Technology, Lausanne, EPFL, where he taught in the field of IC manufacturing. Dr. Fazan has authored or co-authored more than 100 papers and has invented or co-invented more than 190 U.S. patents. Dr. Fazan has served as a member of multiple conference program committees. He obtained his physics diploma and Ph.D. degrees at the Swiss Federal Institute of Technology (EPFL) in 1984 and 1988, respectively. You can reach Dr. Pierre C. Fazan at pfazan@z-ram.com.
of increased density, lower cost and lower power. The spin-torque effect begins to be practical for dimensions below 100nm, and the required current decreases as the area of the bit decreases. With smaller technology nodes becoming increasingly attractive, this and other factors make 65nm the approximate entry point for spin-torque MRAM. Spin-torque MRAM has created broad interest and is currently in development by a number of established and start-up companies.

Key attributes for both types of MRAM result from data being stored as a magnetic polarization. Non-volatility is inherent because magnetization does not leak away with time-like electric charge. Read/write endurance is unlimited because there is no known wear-out mechanism related to switching a magnetic polarization. No matter how many times the magnetic polarization is reversed it always alternates between the same two stable states.

After mapping the capabilities of these emerging technologies, it’s clear that each technology has a place in the system hierarchy; but the most demanding “working memory” applications require fast cycle times and very high (infinite) endurance, pointing to MRAM as the only viable non-volatile candidate in the near term. Additionally, as the family of MRAM products continues to increase in densities while achieving lower costs through the development of next-generation toggle, then spin-torque products, MRAM technology will capture more of the code and data storage segments of the system architecture.

About the Author
Douglas Mitchell is vice president of sales and marketing at Everspin Technologies in Chandler, Arizona. He holds a B.S.E.E. from the University of Texas in Austin and an MBA from National University in San Diego. Mr. Mitchell has more than 30 years of experience in the semiconductor industry.